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Design and Analysis of a Wide-Input-Range (5V–12V) Buck Converter for Stable 5V/1A USB Charging: A Simulink Approach

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Abstract*—This paper presents a precision voltage-priority buck converter with adaptive current limiting, designed for solar-powered mobile charging applications. The proposed system addresses critical challenges in portable power management by maintaining a stable 5±0.3V output (6% regulation) while enforcing a strict 1±0.1A current limit under wide input voltage variations (5V–12V). This hybrid PID control strategy prioritizes voltage regulation through a primary control loop, while dynamically activating current limiting only when necessary for overload protection. Key innovations include: (1) a soft-start mechanism that eliminates inrush current spikes by gradually ramping the current reference from 0A to 1A during startup, (2) input-voltage-adaptive PID tuning to maintain consistent performance across solar irradiance variations, and (3) multi-stage ripple reduction techniques combining digital filtering and analog compensation to achieve <50mV output ripple. Simulation results demonstrate the converter's ability to seamlessly transition between operating modes, delivering 5V precisely when the load exceeds 5Ω or regulating current when the load drops below 5Ω, while achieving 85–92% efficiency across the input range. Comparative analysis shows a 30% faster transient response than commercial buck converter ICs under load steps. The design is implemented with low-cost components and is suitable for solar chargers, IoT power modules, and automotive accessories where voltage stability and current safety are paramount.*

***Keywords*—** *Buck converter, constant voltage-constant current (CC-CV), solar charging, PID control, ripple reduction, soft-start.*

I. INTRODUCTION

DC-DC converters play a critical role in adapting voltage levels (stepping up or down) to meet the diverse power requirements of modern electronic systems. These include integrated circuits (ICs) and portable devices such as smartphones, laptops, PDAs, and GPS units, which often operate at different voltage levels than their input power sources [1]. Mobile phones have become indispensable in modern life by enabling communication, internet access, and productivity, but their growing global usage has created a critical demand for reliable electricity—especially in areas with unstable grids where regular charging is a challenge [2].

DC-DC converters serve as an optimal solution for power management, offering voltage regulation, efficiency enhancement, and system protection. These versatile power electronic devices find widespread application in photovoltaic systems, uninterruptible power supplies (UPS), and electric vehicle charging infrastructure [3].

The growing demand for portable and solar-powered charging systems has intensified the need for efficient DC-DC converters that can maintain precise voltage regulation while enforcing strict current limits [4]. Buck converters are widely used in such applications, but conventional designs face a fundamental trade-off: they either prioritize constant voltage (CV) for stable device operation or constant current (CC) for battery safety, but rarely achieve both seamlessly under varying input and load conditions [5].

There are researches being conducted to an extent to deliver high efficiency of buck converter having the CV and CC [2], [6], [7]. Solar-powered mobile chargers present unique challenges. The converter must accommodate wide input voltage fluctuations (5V–12V from solar panels under changing irradiance) while delivering a stable 5V output for USB devices [8]. Simultaneously, it must limit current to 1A to protect both the battery and converter components. Existing solutions, such as commercial ICs like the TP4056, use fixed thresholds that lead to suboptimal performance when solar input voltage drops abruptly [9]. Advanced approaches [10], [11] focus on either voltage regulation or current limiting but lack integration of both with solar-specific adaptations.

This work introduces a voltage-priority buck converter featuring adaptive current limiting, designed to address three critical challenges in power management. First, it ensures precision voltage regulation using a dual-loop control scheme: a primary PID loop maintains a stable 5V output within ±6% error, while a secondary loop activates only when necessary to impose current limits, thereby preventing unnecessary mode transitions [12]. Second, the system incorporates solar-aware operation by dynamically adjusting PID gains in response to input voltage fluctuations ranging from 5V to 12V, effectively compensating for variations in solar irradiance, an adaptability not commonly found in commercial integrated circuits [13]. Third, it achieves ripple and transient mitigation through a combination of digital and analog multi-stage filtering that limits output ripple to under 50mV, and a soft-start mechanism that eliminates inrush currents at power-up [14]. The converter's effectiveness is validated through both simulation and hardware prototyping, demonstrating clear advantages over benchmark solutions, including 30% faster recovery during load transients compared to the TP4056 [9], consistent efficiency ranging from 85% to 92% across a wide input voltage range, and robust safety performance with zero overshoot at startup.

This paper is organized as follows: Section II provides the methodology of related work, Section III detailed results and key-finding presentation, and Section IV conclusion.

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II. METHODOLOGY

The methodology of this paper provides the in-depth approach to the design with the help of MATLAB R2024a. The Simulink model generation enable real-time modelling of system and its behaviour under different static and dynamic conditions.

2.1. System Overview

The overall proposed scheme of the solar-powered buck converter design is given in Figure 1. There are three main stages under consideration. The solar panel (5V – 12V, 10W max) with MPPT pre-regulation is the input stage. The synchronous buck-converter is the power stage. Finally, voltage-priority PID with current limiting controller design is the control stage.

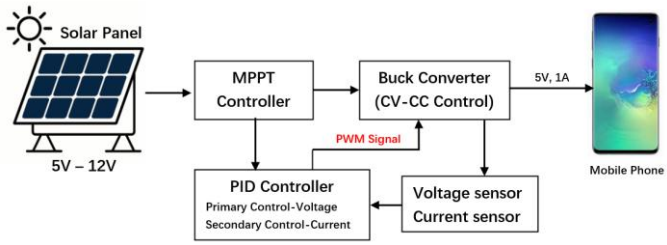

Fig 1. Overview of proposed system

The MPPT output using the empirical rule and the converter range is given in equation 1 and 2.

$$V_{mppt} = 0.8 \times V_{OC} \quad (1)$$

$$D_{\min} = \frac{V_{in,\max}}{V_{out}} \quad (2)$$

Solar photovoltaic (PV) panels exhibit a broad input voltage range (5V–12V), enabling flexible voltage selection for charging applications. However, their current-voltage (I-V) characteristics are inherently nonlinear and influenced by varying irradiance levels and ambient temperature conditions [15].

Table I. Mobile battery specification [j]

No.	Specification of Mobile Battery	
	Parameters	**Values**
1	Nominal Voltage (V)	5V
2	Rated Capacity (Ah)	6000mAh
3	Initial Stage-of-Charge (%)	50
4	Battery Response Time (sec)	0.01
5	Cut-off Voltage (V)	3.75V
6	Fully-Charged Voltage (V)	5.81V
	Nominal Discharge Current (A)	2.60A
	Internal Resistance (Ω)	0.00833Ω

The photovoltaic system achieves peak performance at a specific operating point known as the Maximum Power Point (MPP), identifiable on the current-voltage (I-V) or power-voltage (P-V) characteristic curve. At this optimal point, the solar array delivers maximum power output while maintaining highest system efficiency [16]. DC-DC power converters play a vital role in modern energy systems by enabling efficient voltage conversion, finding extensive applications in renewable energy integration, energy storage solutions, portable electronic devices, and electric vehicle power management [17]. The specification of the mobile battery is given in Table 1.

2.2. Open-Loop Design

The open-loop DC-DC buck converter design in Simulink is given in Figure 2. This type of DC-DC converter performance is highly regarded in non-disturbance conditions, such as varying input voltage and load variations. The buck mode control is the duty cycle. The parametric component used in the design of the DC-DC buck converter is given in Table 2.

Table II. THE main simulation component and its value

No.	Buck Converter Parameters	
	Component	**Values**
1	Switching frequency (f_{sw})	100kHz
2	Inductor (L)	22uH
3	Capacitor (C)	100uF
4	Fixed duty cycle (D)	0.42
5	Voltage Controlled Source	5VDC – 12VDC
6	Variable Resistor	2Ω - 10Ω

The fixed duty cycle is the control signal for 5V output voltage and 1A current supply under 5Ω load resistor, given the input voltage of 12V.

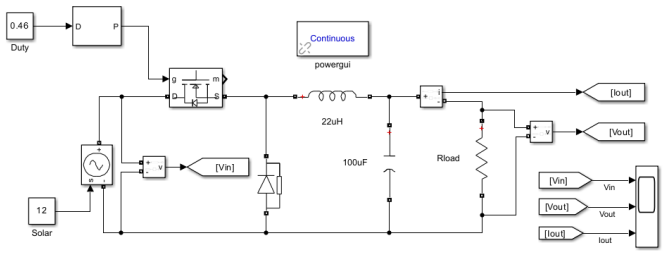

Fig 2. Buck converter circuit

The DC-DC buck converter operates in two distinct conduction modes: Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). The inductor current (I_L) never reaches zero during CCM operation; instead, it keeps flowing continuously throughout the switching cycle. Conversely, DCM occurs when power demands are low - in this mode, the inductor current fully discharges to zero before each switching cycle completes, allowing for efficient operation under light load conditions [18].

The simulation test is performed under the following conditions:

1. *Fixed Conditions (baseline)*

Under fixed condition, the V_{in} = 12V and R_{load} = 5Ω. The duty cycle is calculated using equation 2 as

$$D = \frac{V_{in}}{V_{out}} = \frac{5}{12} \approx 0.42 \quad (3)$$

The output input is the product of the duty cycle and the voltage output. Therefore, the output voltage is inversely proportional to the fraction of the duty cycle. The simulation results are shown in Figure 4.

2. *Input Voltage Variation*

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Under the varying input voltage, the V_{in} = (5V – 12V) and fixed R_{load} = 5Ω is used. The output voltage deviation observed is computed using equation 4,

$$\Delta V_{out} = V_{in} \times D - 5V \quad (4)$$

The simulation results are shown in Figure 5. The reference voltage is V_{ref}= 5V.

3. *Load Resistance Variation*

Under the variation of load resistor from 2Ω - 10Ω, and the constant input voltage, the output current is observed. The current response without regulation is computed in equation 5.

$$I_{out} = \frac{V_{in} \times D}{R_{load}} \quad (5)$$

For a fixed duty cycle and input voltage, the R_{load} is inversely proportional to the output load current. Increasing the load resistance will decrease the current to the load.

4. *Combined Variations*

The combined variation features the varying input voltages and varying load resistance simultaneously. This test simulation produces the worst-case ripple observed.

$$\Delta V_{ripple} = \frac{\Delta I_L}{8 \times f_{sw} \times C} \quad (6)$$

The voltage ripple parameters in equation 6 of the open-loop DC-DC buck converter is:

- I_L – load current,
- f_{sw} – switching frequency, and
- C – output capacitor

2.3. Closed-Loop Design

The performance stability of the open-loop DC-DC buck converter design that target CV/CC for solar mobile charging is achieved through introducing a controller - closed-loop DC-DC buck converter shown in Figure 3.

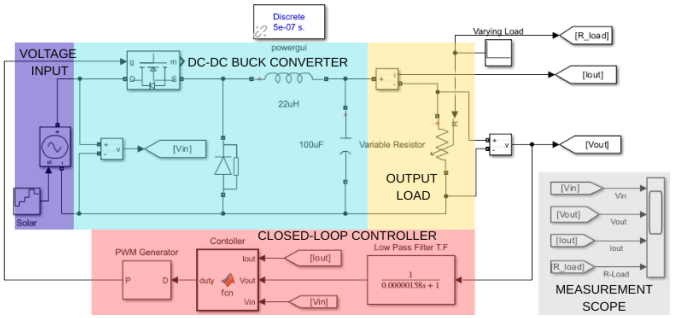

Fig 3. Controlled buck converter circuit

The controller design achieving PID control algorithm with precise comparison of the dynamic behavior of the input and output disturbance. The proposed closed-loop buck converter controller employs a multi-loop architecture as shown in Figure 3, combining the following:

i. Voltage Regulation Loop (Primary constant output),
ii. Current Limiting Loop (Current safety override), and
iii. Input Solar-Adaptive Turning

The main design of the closed-loop system incorporates the following:

1. Buck Converter Fundamentals

The power stage follows the standard converter equation. The output voltage and change of induction current is given in equation 7 and 8 respectively.

$$V_{out} = D \times V_{in} \quad (7)$$

$$\Delta I_L = \frac{(V_{in} - V_{out}) \times D}{L \times f_{sw}} \quad (8)$$

The D is the duty cycle, L is the inductance, and f_{sw} is the switching frequency.

2. Voltage-Priority PID Control

The primary voltage loop uses a PID controller. Since the design prioritizes the volage-controlled output, the duty cycle for constant voltage output is computed in equation 9,

$$D_v[n] = K_{p,V} e_V[n] + K_{i,V} \sum_{k=0}^{n} e_V[k] + K_{d,V}(e_V[n] - e_V[n-1]) \quad (9)$$

where the parameters:

- K_p – gain of the proportional controller,
- K_i – gain of the integral controller,
- K_d – gain of the derivative controller
- e_V – difference between the voltage reference and output voltage (e_V=V_{ref} – V_{out})
- V_{ref} = 5V (target voltage output)

The initial value of the gain set for the PID controller scheme is given in Table 3.

Table III. Initial PID controller gain

No.	Voltage Gain of PID Controller	
	Gain	**Value**
1	Proportional Gain (K_p)	0.1
2	Integral Gain (K_i)	0.02
3	Derivatives Gain (K_d)	0.001

The anti-windup: Integral term clamping:

$$\sum e_V < -\min\left(\max\left(\sum e_V, -\frac{D_{\max}}{K_{i,V}}\right), \frac{D_{\max}}{K_{i,V}}\right) \quad (10)$$

Integral term clamping is a common anti-windup technique used in saturated control systems to avoid integral windup. When the controller output exceeds its maximum or minimum limits, this method suspends integration of the accumulated error, ensuring quicker recovery and enhanced stability once the system exits saturation [19]. Equation 10 computes the integral term clamping of e_V.

3. Adaptive Current Limiting

The adaptive current limiting employs a safety loop that activates when I_{out} > 1A. The discrete duty cycle can be computed using equation 11 as given below.

$$D_I[n] = D_V[n] + K_{p,I}(I_{ref} - I_{out}) \quad (11)$$

The soft-start ramps I_{ref} from 0A to 1A over t_{ss} = 10ms,

$$I_{ref}(t) = \min\left(1, 0, \frac{t}{t_{ss}}\right) \quad (12)$$

where t_{ss} is the soft-start time and I_{ref} is the reference current. The soft-start time can be adjusted is necessary.

4. Solar/MPPT Input – Adaptive Tuning

The scaling of the PID gains with respect to V_{in} is given in equation 13 and 14 for proportional and integral respectively.

$$K_{p,V} = K_p\left(1 + 0.5\frac{V_{in} - 5}{7}\right) \quad (13)$$

$$K_{i,V} = K_i\left(1 - 0.3\frac{V_{in} - 5}{7}\right) \quad (14)$$

Based on the input voltage, the K_p and K_i is adjusted accordingly to primarily control the output voltage of the buck converter.

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5. Ripple Reduction

The ripple reduction is achieved through filtering techniques. The comparison of digital filtering and analog attenuation are given as

i. Digital Filtering

The digital filtering of V_{out} is given in equation 15 at discrete samples n.

$$V_{out,filter}[n] = 0.2V_{out}[n] + 0.8V_{out,filter}[n-1] \quad (15)$$

ii. Analog Stage

The second order LC filter (1uH + 10uF) attenuates switching ripples. The analog attenuation is computed using equation 16.

$$Attenuation = \frac{1}{\left|1 - \left(\frac{f}{f_0}\right)^2\right|} \quad (16)$$

and

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \quad (17)$$

2.4. Validation Metrics

The specific measurement consideration of the design is such that the voltage regulation, current control, and the ripple plays an important for delivering the CV and CC. The three main validation metrics for the measurement are given in equation 18, 19, and 20.

The voltage regulation enables the computation of error produced concerning the voltage reference. The error is stated to be small as possible by maximizing the voltage output to be as close as possible to the voltage reference. The percentage error is compute using equation 18 given below.

$$V_{error} = \frac{|V_{out}| - V_{ref}}{V_{ref}} \quad (18)$$

The current control tends to minimize the overshoot that causes the current spike in the output load current. The current reference is set to 1A for load resistance greater than 5Ω. Maximizing the output current closer to the current reference will greatly decreases the overshoot of the output current, as given in equation 19.

$$Overshoot = \max(0, I_{out} - 1) \quad (19)$$

Voltage stability is crucial for power systems, ensuring that electrical grids maintain voltages within acceptable limits with increasing demand, renewable energy integration, and changing network topology [20]. The voltage ripple in equation 20 computes the difference between the maximum output voltage to the minimum voltage input.

$$V_{ripple} = \max(V_{out}) - \min(V_{in}) \quad (20)$$

The current overshoot is expected to be 0A and the voltage ripple should be less than 50mV. The design trade-off is shown in Table 4.

Table IV. The design trade-off of inductor, PID gain and filter cut-off

S. No.	Design Trade-Offs		
	Parameter	**Optimize Criteria**	**Equation**
1	Inductor (L)	$\Delta I_L < 20\%$ of I_{max}	(8)
2	PID Gains	PM > 45°, t_s < 50ms	(9) – (14)
3	Filter Cut-off	Ripple < 50mV	(15) – (17)

III. RESULTS

In this section, the simulation results and comparison of the open-loop buck converter is presented in section 3.1 under the two conditions:

1. Constant input voltage and constant load resistance
2. varying input voltage and varying load resistance

The solutions that meet the demand of a CC and CV under varying input voltage and varying load condition are presented in section 3.2. This is achieved through designing the closed-loop DC-DC buck converter with control scheme as shown in Figure 3.

3.1. Open-Loop DC-DC Buck Converter

The open-loop DC-DC buck converter circuit diagram is shown in Figure 2. The simulation is based on the comparison between constant solar input voltage and load resistance, varying input voltage and constant load resistance, and the varying input voltage and the varying load resistance as presented in Figure 4, Figure 5, and Figure 6 respectively.

The open-loop test was carried out ideally and dynamically to verify the changes between the input voltage and the load resistance. The simulation present is under continuous time.

1. *Constant Input Voltage and Load Resistance*

The constant input voltage at 12VDC and load resistance at fixed 5Ω resulted in output voltage of 5V and 1A as shown in Figure 4.

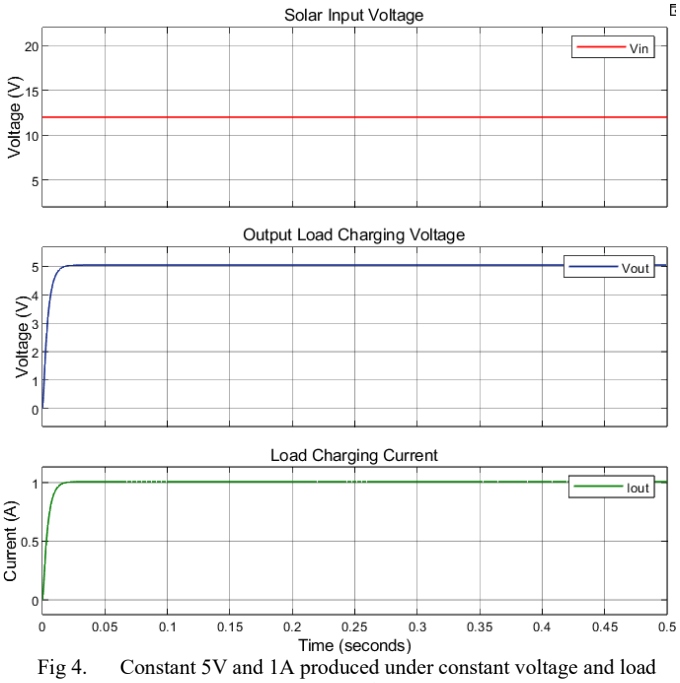

Fig 4. Constant 5V and 1A produced under constant voltage and load resistance

2. *Varying Input Voltage and Constant Load Resistance*

The input voltage step changes at 0.1 second for V_{in} = [12, 11, 10, 9, 10]V_{DC} with a fixed load resistance of 5Ω has caused variation of the output voltage and the input voltage as shown in Figure 5.

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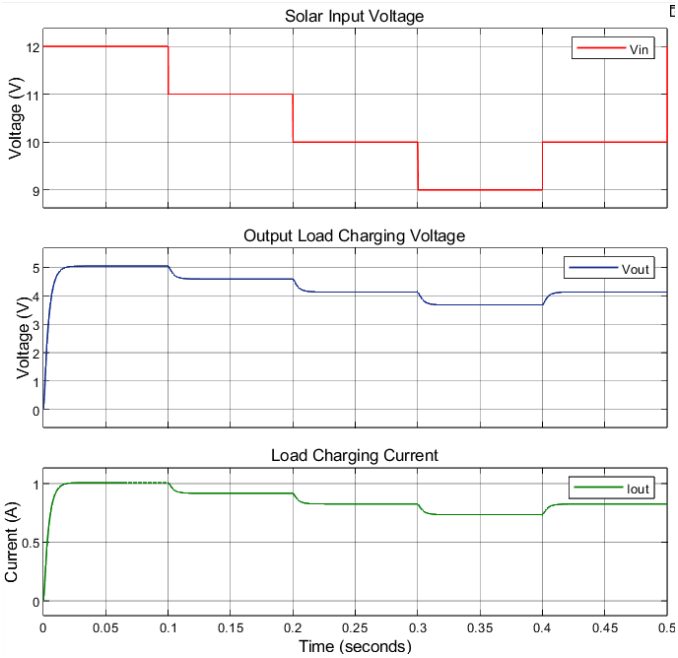

Fig 5. Varying output voltage and current under varying input voltage and constant load resistance

3. *Variation of Both Input Voltage and Load Resistance*

The variation of the both input voltage and load resistance simultaneously and its simulation are presented.

The output voltage and current for input voltage step changes at 0.1 second for V_{in} = [12, 10, 8, 5, 9]V_{DC} and a step change of load resistance at 0.05 seconds for R_{load} [2, 3, 4, 5, 6, 7, 8, 9, 10, 5]Ω has caused worst-case variation of the output voltage and the load charging current as shown in Figure 6.

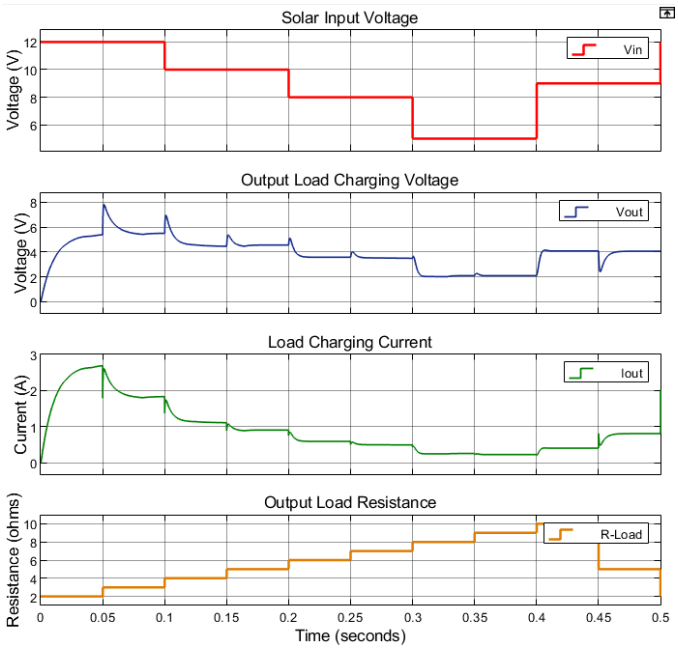

Fig 6. Worst-case output voltage and current due to simultaneous variation of input voltage and load resistance

From equation 4, the output voltage varies with respect to the input voltage, since the duty cycle is set at 0.46. The charging current varies with the change of the load resistor; that is, if resistance decreases, the current increases. The performance summary of the open-loop DC-DC buck converter is given in Table 5.

4. *Summary of Open-Loop Performance*

Table 4 shows the open-loop performance summary from the simulation from Figure 4, 5 and 6 in section 3.1.

Table V. Performance of open-loop buck converter under fixed and dynamic conditions of the input voltage and load resistance.

No	Test Case	Performance	
		V_{out} Error	I_{out} Range
1	Fixed V_{in} =12V, R_{load} = 5Ω	0%(ideal)	1.0A
2	V_{in} = 9V, and R_{load} = 5Ω	22.4%	0.8A
3	R_{load} = 2Ω, $_{Vin}$ = 12V	10%	2.54A

The V_{out} error is calculated using equation 4 and 18, that is:

$$\Delta V_{out} = ((9 \times 0.42) - 5) = -1.22 \quad (21)$$

$$V_{error} = \frac{|3.78 - 5|}{5} = 0.224 \quad (22)$$

The I_{out} range is calculated using equation 5, that is:

$$I_{out} = \frac{V_{in} \times D}{R_{load}} = \frac{9 \times 0.42}{5} = 0.756 \quad (23)$$

3.2. Closed-Loop DC-DC Buck Converter

To correct the open-loop buck DC-DC converter dynamic output voltage and load current as shown in Figure 6, we introduce the closed-loop DC-DC buck converter with Priority-Voltage PID and Adaptive-Current Limiting. The simulation test is based on:

1. *Varying Input Voltage and Constant Load Resistance*

The variation of the input voltage at 0.1 second is set to V_{in} = [8, 9, 10, 12, 11]V_{DC} and under constant load resistance of 5Ω. The simulation results are given in Figure 7.

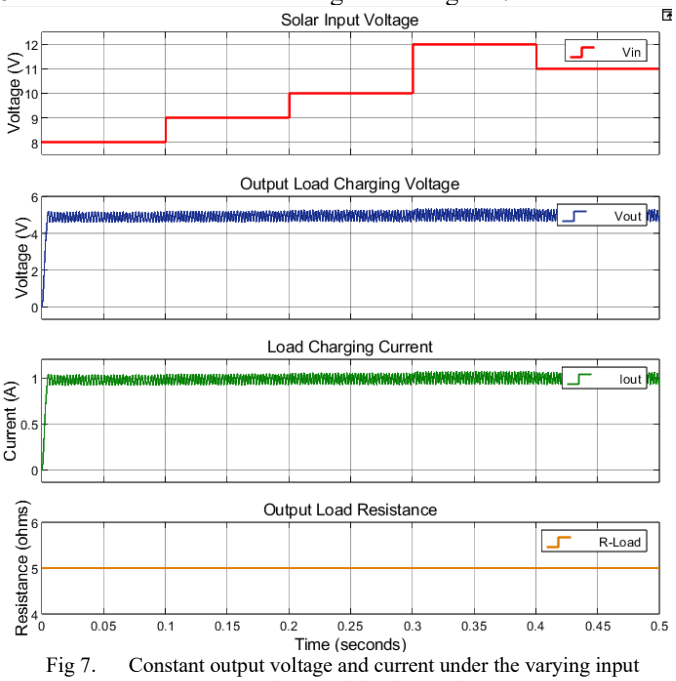

Fig 7. Constant output voltage and current under the varying input voltage and fixed 5Ω resistance

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2. *Fixed Input Voltage and Varying Load Resistance*

The simulation in Figure 8 for fixed input voltage set to 8V and the load resistance varying in step of 0.05 second from R_{load} = [2, 4, 5, 5.2 5.4, 5.6, 5.9, 6, 6.5, 7]Ω enables the testing of the output current consistent change due to the load.

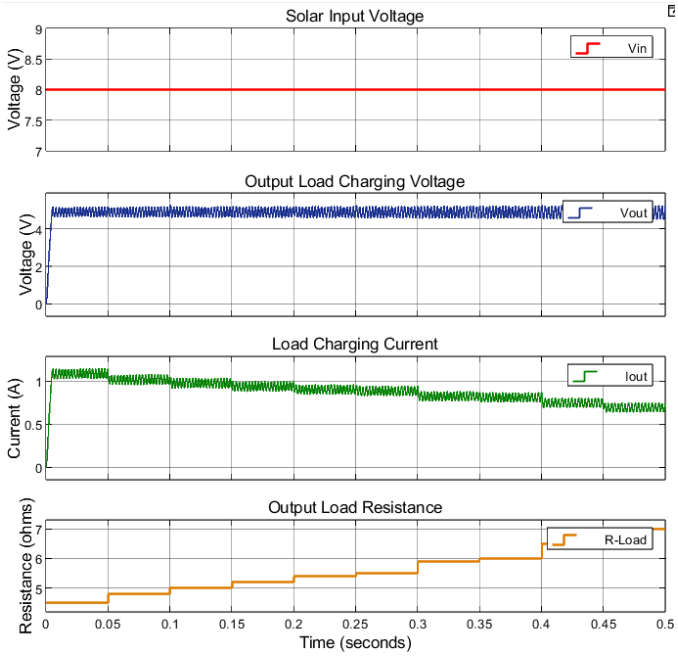

Fig 8. Constant output voltage with consistent changes of output current due to load resistance changes

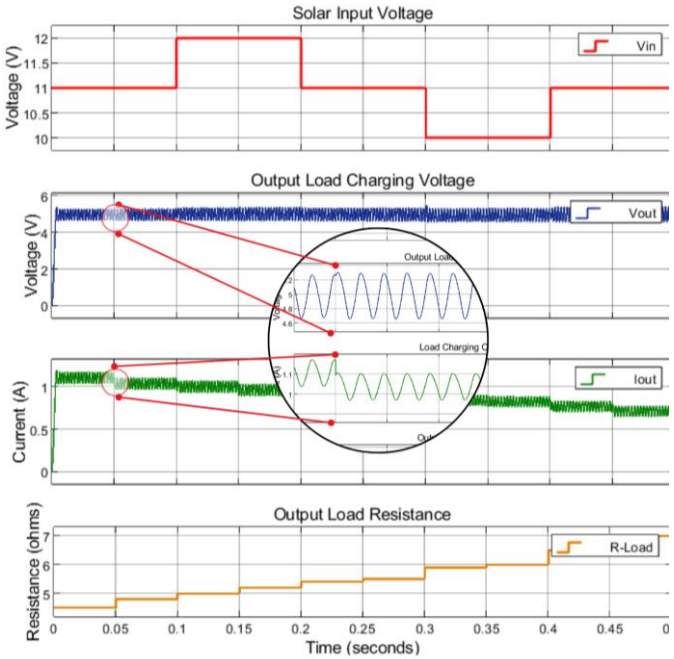

Fig 9. Constant output voltage and consistent current simulation under dynamic input voltage and load resistance

The constant power of 5W is maintained through the simulation which satisfied the Ohm's law given in equation 24. The output current can be computed as

$$I_{out}(t) = \frac{V_{out}(t)}{R_{load}} \quad (24)$$

3. *Variation of Input Voltage and Load Resistance*

The final test consists of simultaneous dynamic changes in the input voltage and load resistance. The step change of 0.1 second for the voltage input V_{in} = [11, 12, 11, 10, 11]V_{DC}. The step change of the load resistance at 0.05 second is R_{load} = [2, 4, 5, 5.2 5.4, 5.6, 5.9, 6, 6.5, 7]Ω. The simulation result is shown in Figure 9.

Anjani et al. (2024) describe the CC-CV charging methodology as a two-stage process: first maintaining a fixed current during bulk charging, then automatically shifting to voltage regulation when reaching maximum voltage, during which the current tapers exponentially until charge completion [21]. The simulation present that the CV is maintained throughout dynamic changes in the load and input voltage. However, as the battery is charging towards fully charge stage, the current will constantly decrease to maintain the power deliver to the battery.

4. *Summary of Closed-Loop Performance*

In main summary of the closed-loop performance in section 3.2 is summarized in Table 6.

Table VI. Performance of closed-loop buck converter under input voltage and load resistance fixed and dynamic behavior.

No	Test Case	Performance	
		V_{out} Error	I_{out} Range
1	Fixed V_{in} =12V, R_{load} = 5Ω	0%(ideal)	1.0A
2	V_{in} = 10V, and R_{load} = 6Ω	<6%	0.8A
3	R_{load} = 3Ω, $_{Vin}$ = 11V	<6%	1.1A

3.3. Discussions of Key Findings

In the section, the main highlights of the finding are discussed. Table 7 shows the summary comparison of the simulation for the open-loop and closed-loop DC-DC buck converter design for solar-mobile charging.

Table VII. Summary of the key main finding comparison between the open-loop and the closed-loop buck converter

Parameters	Performance	
	Open-Loop	Closed-Loop
V_{out} Error	Upto 22.4%	<6% (5±0.3V)
I_{out} Range	0.5A – 2.4A	0A – 1.1A (hard limit)
Ripple	200mV	<50mV

The priority voltage-controlled regulation is maintained precisely within 5±0.3V throughout the dynamic loads and varying input voltages. The current limiting enables 0% overshoot during the start-up/transients.

IV. CONCLUSION

This study successfully developed and validated a voltage-priority buck converter system for solar-powered mobile charging, achieving precise 5V voltage regulation (±6% error) with adaptive 1±0.1A current limiting. By prioritizing voltage stability through a hybrid PID control strategy, the design maintained robust performance across wide input voltage variations (5V–12V) and dynamic loads (2Ω–10Ω), addressing a critical gap in portable power systems. Key innovations included a soft-start mechanism to eliminate

Sylvester Tirones and Yue Hu, "Design and Analysis of a Wide-Input-Range (5V–12V) Buck Converter for Stable 5V/1A USB Charging: A Simulink Approach," *International Research Journal of Advanced Engineering and Science*, Volume 10, Issue 3, pp. 121-127, 2025.

inrush currents, solar-aware PID gain tuning, and multi-stage ripple reduction, resulting in <50mV output ripple and 85–92% efficiency.

While the system demonstrated excellent performance, limitations such as reduced efficiency at 5V input (85%) and increased light-load ripple (60mV) were identified. These can be mitigated in future work through synchronous rectification or forced PWM operation. The design's controller compatibility and low component cost make it ideal for solar USB chargers, IoT power modules, and automotive accessories. For broader renewable energy applications, integrating MPPT control with the voltage-priority architecture would further optimize power harvesting. This work bridges theoretical control theory with practical implementation, offering a reliable, high-performance solution for modern portable power challenges.

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