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Design & Simulation of Nanoscale Single & Double Gate MOS Structures with High-k Gate Oxide using Ballistic Transport Model

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***Abstract*—** *The scaling of the MOSFET continues to sustain Moore's law and reaches the nanometer regime. The dimensions of modern transistors are getting closer to the electron mean free path, which increases the relevance of ballistic transport. With the scaling in the channel length, the carrier transport phenomenon approaches to ballistic limit. In this work, the electrical performance of ballistic single-gate and double-gate MOS structures with 10 nm Si body thickness is studied. For both the MOS structures HfO_2 as high-k gate oxide material is used. The FETToy simulation tool is used to simulate the I-V characteristics. The simulated results of the single-gate and double-gate MOSFETs are compared. The impact of gate oxide thickness on its I_d - V_g characteristics and quantum capacitance (C_Q) is explored. It has been found that the double-gate MOS structure exhibits higher drain current and higher quantum capacitance value as compared to the single-gate structure. The on-current is higher for the double gate MOSFET which enables a faster switching speed and is beneficial for memory devices.*

***Keywords*—** *Ballistic model:High-k:MOS: Quantum Capacitance.*

I. INTRODUCTION

The small size of MOSFETs has become one of the most essential devices in the semiconductor industry due to their successful integration into integrated circuits (ICs). The size of MOSFETs has consistently reduced by a factor of two every two years, even though their physical structure has not changed entirely [1, 2]. In the sub-10 nm channel region, the control of the gate on the channel starts degrading due to enhanced short-channel effects. These effects are Drain-Induced Barrier Lowering, velocity saturation, hot-carrier effect, surface punch-through, threshold voltage roll-off, etc. [3]. The continuous scaling of single gate MOSFET is challenged by the physical limitation of silicon and the gate dielectric, leading to issues like gate oxide breakdown and increased gate leakage [4]. As gate oxide thickness is reduced, leakage current arises due to the tunneling of carriers. CMOS technology which uses SiO_2 as an insulator material has reached its maximum limit [5]. Shorter channels lead to higher leakage currents because the gate can only control the channel from one side and hence consume more power. Due to these limitations, alternative multi-gate MOSFET structures have been explored. The double gate transistor structure is one of the promising choices for nano regime devices. It has two gates that control the channel from both sides, providing superior control over the channel. The device's performance is enhanced by the double gate structure's higher electrostatic control of the gate across the channel, which lowers short-channel effects. In short channel MOSFETs, for both high-performance and low-power applications, high-k gate oxide is proving to be an alternative to traditional SiO_2 gate oxide [6]. There are many high-k materials for gate oxide such as HfO_2, Al_2O_3, ZrO_2, La_2O_3, etc. In this study, HfO_2 is utilized as a gate oxide material because of its excellent balance of high dielectric constant, thermal stability, chemical stability, and compatibility with silicon technology [7]. This paper compares the electrical performances of single gate and double gate MOS structures with 10 nm Si body thickness. Quantum capacitance is an important factor in nanoscale MOSFET as it affects various performance parameters of the device like threshold voltage, gate capacitance, and overall electrical characteristics. Therefore, in this work, the device performance parameters drain current and quantum capacitance are examined for both MOS structures.

II. DEVICE STRUCTURE & SIMULATION METHOD

The two device structures single gate and double gate MOSFET considered in this work are depicted in Fig.1. The single gate MOSFET consists of a source, drain, and single gate terminal, whereas double gate MOSFET has two gate terminals gate 1 and gate 2. The gate oxide thickness is represented by T_{ox}. The Silicon body thickness of both the structures used is the same (T_{Si} = 10 nm). The metal contacts are made at the drain, source, and gate terminals to apply the biasing to the device. The various design parameters and their values used in the simulation are given in Table 1. The biasing is applied at the drain and gate terminals w.r.t. the source. The biasing voltage is divided into 12 bias points with a starting value of 0 V and a final value of 1 V. The source terminal is kept at 0 V. Silicon is taken as channel material whose valley degeneracy value is 2 [8]. The FETToy simulator tool is used to simulate device characteristics [9]. As the size of the transistors becomes smaller and reaches the nanoscale, traditional diffusive transport models become less accurate. Since electrons can travel in a ballistic manner, the carrier scattering events in these ultra-small devices are decreased. Therefore, ballistic transport can reduce energy loss and increase efficiency in electrical systems while also improving speed [10]. The 2-dimensional model of ballistic MOSFET is depicted in Fig. 2. Due to potential barriers, the effect of three capacitors drain capacitance (C_D), source capacitance (C_S), and gate capacitance (C_G) is considered in this simulation. The mobile charges are calculated by the source and drain Fermi

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levels location, the local density of states D(E), and self-consistent potential (U_{scf}). Unlike classical oxide capacitance which depends on the physical dimensions and dielectric properties of the capacitor, quantum capacitance (C_Q) depends upon the electronic structure and density of states in the material.

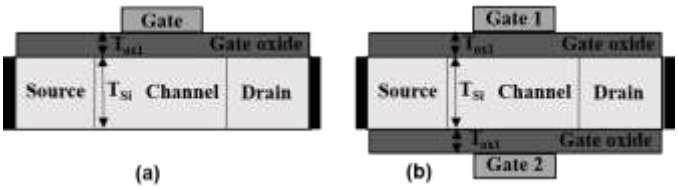

Fig. 1. Schematic diagram of device structures used in the simulation (a) Single Gate MOSFET, (b) Double Gate MOSFET

TABLE I. Design parameters used in the simulation.

Input parameters are given in the simulator		Symbol	Values
Oxide thickness		t_{ox}	2 nm - 8 nm
Insulator dielectric constant		ε_{ox}	25
Threshold voltage		V_t	0.30 (V)
Valley Degeneracy		N_v	2
Temperature		T	300 (K)
Gate control parameter		α_G	0.88
Drain control parameter		α_D	0.035
Si Body Thickness		T_{si}	10 nm
Effective Mass ratio		m^*/m_o	0.19
Doping Density		N_d	1×10^{20} (/cm3)
Gate	Initial voltage	V_g	0(V)
	Final voltage	V_g	1(V)
	Number of bias points	-	12
Drain	Initial voltage	V_d	0 (V)
	Final voltage	V_d	1 (V)
	Number of bias points	-	12

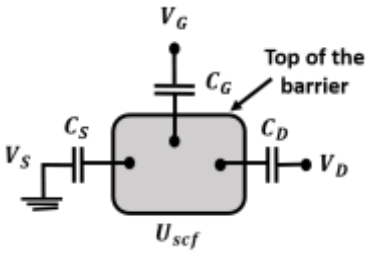

Fig. 2. 2-D model of ballistic MOSFET

In equilibrium, the quantum capacitance is calculated as [11].

$$C_Q = q^2 \int_{-\infty}^{+\infty} D(E) \left(-\frac{\partial f\,(E-E_F)}{\partial E}\right) dE \qquad (1)$$

when all the biasing voltages are zero, the electron density in equilibrium is

$$N_0 = \int_{-\infty}^{+\infty} D(E)\, f(E - E_F) dE \qquad (2)$$

when the biasing voltage is given to the drain and gate terminals, and the source is grounded, the density of states is filled by the two Fermi levels. The source and drain are filled by the positive and negative velocity states respectively which are given by

$$N_1 = \frac{1}{2}\int_{-\infty}^{+\infty} D(E) f_1(E)\, dE \qquad (3)$$

$$N_2 = \frac{1}{2}\int_{-\infty}^{+\infty} D(E) f_2(E)\, dE \qquad (4)$$

where

$$f_1(E) = f(E + U_{scf} - E_{f_1})$$
$$f_2(E) = f(E + U_{scf} - E_{f_2})$$

The total electron density is $N = N_1 + N_2$. The self-consistent potential is given by

$$U_{scf} = -q(\alpha_G V_G + \alpha_D V_D + \alpha_S V_S) + U_C \Delta N \qquad (5)$$

where

$$\alpha_G = \frac{C_G}{C_\Sigma}\ ,\ \alpha_D = \frac{C_D}{C_\Sigma}\ ,\ \alpha_S = \frac{C_S}{C_\Sigma}$$
$$U_C = \frac{q^2}{C_\Sigma}\ ,\quad \Delta N = (N_1 + N_2) - N_0$$

where E_{f_1} = Fermi level at the source, E_{f_2} = Fermi level at the drain, q = charge of the electron, α_G = gate control parameter, α_D = drain control parameters, α_S = source control parameter, V_G, V_D & V_S = gate, drain & source voltage, C_Σ = parallel combination of the C_G, C_D, C_S, U_C = charging energy.

The drain current (I_d) in this ballistic model is given by

$$I_d = \int_{-\infty}^{+\infty} J(E)[f_1(E) - f_2(E)] dE \qquad (6)$$

where $J(E)$ is the current density of states [11].

III. Results & Discussion

The simulation results of single gate MOSFET and double gate MOSFET are discussed in this section. The impact of gate voltage (V_g) on the drain current (I_d) and quantum capacitance is studied. The I_d-V_g curve and C_Q-V_g curves are plotted with the help of the FETToy simulation tool. The drain current values at each biased point (0-1 V) are given in Tables 2 and 3 for single and double gate MOSFETs. Fig. 3 (a) and (b) show the I_d-V_g curves for the single gate MOSFET and double gate MOSFET respectively. It is noted from the graphs that with the increase in the gate voltage the drain current increases. Also, it is indicated from the graphs that by decreasing the gate oxide thickness, there is an increase in the drain current for both the MOS structures. From Tables 2 & 3, it is noted that the drain current is almost the same when the voltage at the gate is very low for both MOS structures.

TABLE 2. Variation of Drain Current (I_d) with Gate Voltage (V_g) at different gate oxide thicknesses for Single Gate MOSFET.

Gate voltage (V)	Drain Current (μA/μm)			
	t_{ox} = 2 nm	t_{ox} = 4 nm	t_{ox}= 6 nm	t_o = 8 nm
0	0.014	0.014	0.014	0.014
0.09	0.32	0.32	0.32	0.319
0.18	6.92	6.8	6.69	6.59
0.27	109	92	80.6	72.3
0.36	595	406	314	258
0.45	1500	927	672	529
0.54	2750	1610	1130	864
0.63	4300	2420	1660	1250
0.72	6080	3380	2270	1690
0.81	8050	4460	2960	2180
0.90	10200	5630	3720	2710
1	12500	6890	4540	3290

But after the threshold voltage, the drain current starts increasing and becomes approximately twice as in double gate MOSFET in comparison to single gate MOSFET. This is because, in the deep nanoscale regime, the double gate MOSFET has higher conductivity than the single gate

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MOSFET.

TABLE 3. Variation of Drain Current (I_d) with Gate Voltage (V_g) at different gate oxide thicknesses for Double Gate MOSFET.

Gate voltage (V)	Drain current (μA/μm)			
	t_{ox} = 2 nm	t_{ox} = 4 nm	t_{ox} = 6 nm	t_{ox} = 8 nm
0	0.014	0.014	0.014	0.014
0.09	0.32	0.32	0.32	0.32
0.18	6.97	6.92	6.86	6.8
0.27	121	109	99.5	92
0.36	793	595	480	406
0.45	2180	1500	1150	927
0.54	4140	2750	2030	1610
0.63	6540	4300	3120	2420
0.72	9280	6080	4400	3380
0.81	12300	8050	5810	4460
0.90	15700	10200	7350	5630
1	19300	12500	9010	6890

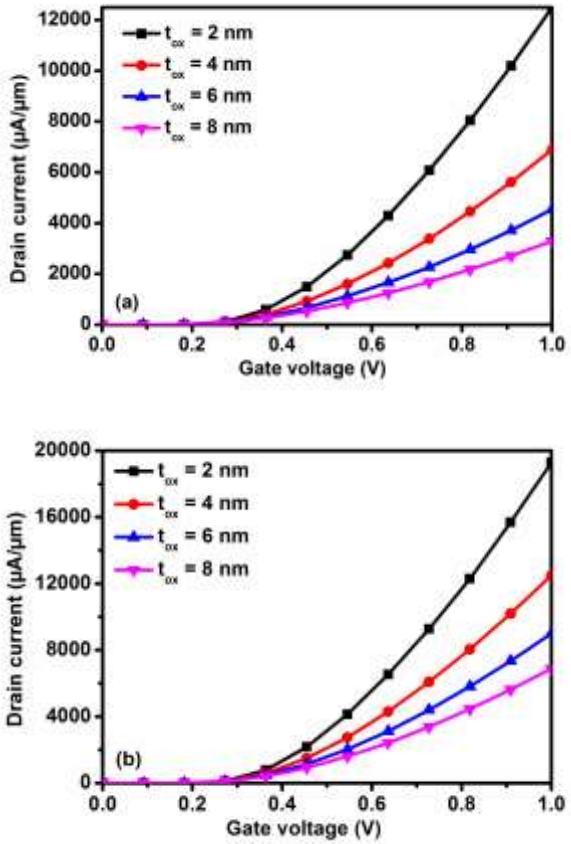

Fig. 3. Drain Current - Gate Voltage (I_d-V_g) curve at different gate oxide thicknesses (a) SG MOSFET, (b) DG MOSFET.

The quantum capacitance versus gate voltage (C_Q-V_g) curve is shown in Fig. 4. (a) and (b) respectively. The C_Q values at each biased point (0-1 V) are given in Tables 4 and 5 for both MOSFET structures. The C_Q -V_g curves are simulated at different oxide thicknesses to analyze the effect of oxide thickness on the quantum capacitance. From Fig. 4, it can be noted that by increase in thickness of gate oxide, C_Q decreases, but is almost constant at initial and higher gate voltages in both the MOS structures.

TABLE 4. Variation of Quantum Capacitance (C_Q) with Gate Voltage (V_g) at different gate oxide thicknesses for Single Gate MOSFET

Gate voltage (V)	Quantum Capacitance (F/cm^2)			
	t_{ox} = 2 nm	t_{ox} = 4 nm	t_{ox} = 6 nm	t_{ox} = 8 nm
0	4.56×10^{-10}	4.56×10^{-10}	4.56×10^{-10}	4.56×10^{-10}
0.09	1.00×10^{-8}	1.00×10^{-8}	1.00×10^{-8}	9.99×10^{-9}
0.18	2.14×10^{-7}	2.10×10^{-7}	2.07×10^{-7}	2.04×10^{-7}
0.27	2.90×10^{-6}	2.51×10^{-6}	2.23×10^{-6}	2.03×10^{-6}
0.36	9.03×10^{-6}	7.47×10^{-6}	6.40×10^{-6}	5.63×10^{-6}
0.45	1.19×10^{-5}	1.06×10^{-5}	9.50×10^{-5}	8.56×10^{-6}
0.54	1.26×10^{-5}	1.20×10^{-5}	1.12×10^{-5}	1.04×10^{-5}
0.63	1.27×10^{-5}	1.25×10^{-5}	1.20×10^{-5}	1.15×10^{-5}
0.72	1.28×10^{-5}	1.27×10^{-5}	1.24×10^{-5}	1.21×10^{-5}
0.81	1.28×10^{-5}	1.27×10^{-5}	1.26×10^{-5}	1.24×10^{-5}
0.90	1.28×10^{-5}	1.28×10^{-5}	1.27×10^{-5}	1.26×10^{-5}
1	1.28×10^{-5}	1.28×10^{-5}	1.27×10^{-5}	1.27×10^{-5}

TABLE 5. Variation of Quantum Capacitance (C_Q) with Gate Voltage (V_g) at different gate oxide thicknesses for Double Gate MOSFET

Gate voltage (V)	Quantum Capacitance (F/cm^2)			
	t_{ox} = 2 nm	t_{ox} = 4 nm	t_{ox} = 6 nm	t_{ox} = 8 nm
0	4.56×10^{-10}	4.56×10^{-10}	4.56×10^{-10}	4.56×10^{-10}
0.09	1.00×10^{-8}	1.00×10^{-8}	1.00×10^{-8}	1.00×10^{-8}
0.18	2.15×10^{-7}	2.14×10^{-7}	2.12×10^{-7}	2.10×10^{-7}
0.27	3.17×10^{-6}	2.90×10^{-6}	2.68×10^{-6}	2.51×10^{-6}
0.36	1.01×10^{-5}	9.03×10^{-6}	8.17×10^{-6}	7.47×10^{-6}
0.45	1.24×10^{-5}	1.19×10^{-5}	1.12×10^{-5}	1.06×10^{-5}
0.54	1.27×10^{-5}	1.26×10^{-5}	1.23×10^{-5}	1.20×10^{-5}
0.63	1.28×10^{-5}	1.27×10^{-5}	1.26×10^{-5}	1.25×10^{-5}
0.72	1.28×10^{-5}	1.28×10^{-5}	1.27×10^{-5}	1.27×10^{-5}
0.81	1.28×10^{-5}	1.28×10^{-5}	1.28×10^{-5}	1.27×10^{-5}
0.90	1.28×10^{-5}	1.28×10^{-5}	1.28×10^{-5}	1.28×10^{-5}
1	1.28×10^{-5}	1.28×10^{-5}	1.28×10^{-5}	1.28×10^{-5}

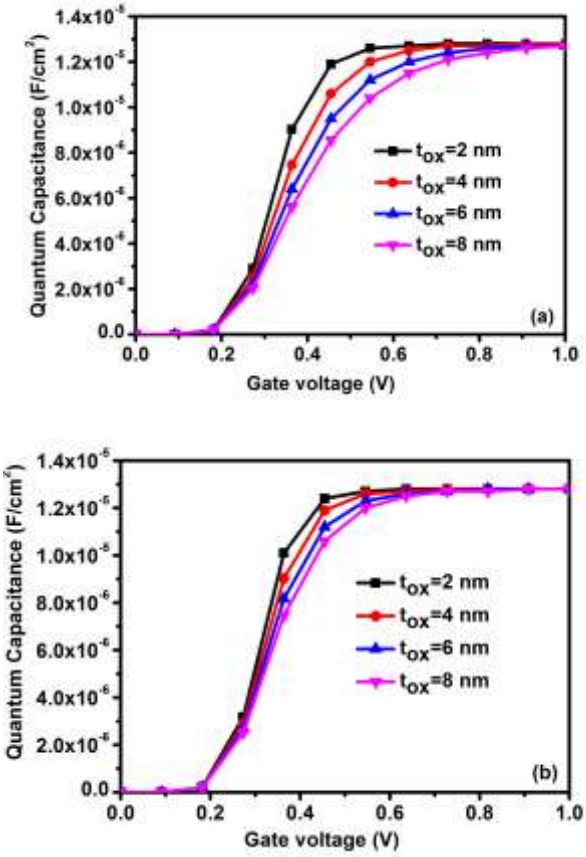

Fig. 4. Quantum Capacitance - Gate Voltage (C_Q-V_g) at different gate oxide thicknesses. (a) SG MOSFET, (b) DG MOSFET

Suruchi Saini and Hitender Kumar Tyagi, "Design & Simulation of Nanoscale Single & Double Gate MOS Structures with High-k Gate Oxide using Ballistic Transport Model," *International Research Journal of Advanced Engineering and Science*, Volume 9, Issue 3, pp. 45-48, 2024.

In nanoscale MOSFET, the total capacitance seen by the gate is a combination of oxide capacitance and quantum capacitance of the channel. Since quantum capacitance is affected by the gate oxide thickness as observed in the graphs, therefore it will also influence the total gate capacitance which will impact the overall gate control over the channel. Further quantum capacitance also affects the threshold voltage of the device and carrier mobility which in turn affects the drive current and switching characteristics of the MOSFET. Hence, by using high-k gate oxide and double-gate configuration, the drain current is increased and quantum capacitance is increased, which helps in making the faster device. Hence, it can be said that DG MOSFET performance is superior to SG MOSFET for 10 nm Silicon body thickness.

IV. Conclusion

This research study presents the simulation of ballistic Single Gate (SG) and Double Gate (DG) MOSFET for 10 nm Si body thickness. The high-k gate oxide (HfO_2) having different thicknesses is used for the simulation of SG and DG MOSFET. The findings indicate that the DG MOSFET outperforms the SG MOSFET. From the I_d-V_g curves, it is concluded that the drain current in DG MOSFET is around double the single-gate MOSFETs for different values of gate oxide thicknesses. Hence, double gate MOSFET has greater on-current which is helpful in fast switching speed. Quantum capacitance vs. gate voltage curves for single-gate and double-gate MOSFETs are also modeled. The graphs demonstrate that as gate oxide thickness increases, the quantum capacitance decreases. Also, DG MOSFET is faster due to the increase in quantum capacitance, which also results in a reduction in propagation delay. As a result, it can be concluded that the double gate MOSFET structure has better quantum capacitance and higher on-current which makes the device faster and improves the overall performance with better switching speed. Hence, this double gate MOS structure can be used in memory devices like SRAM, DRAM, flash memory, and non-volatile memory technologies.

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