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Machine Noise Detection and Filtering using Field-Programmable Gate Array – A Solution to Used Low-end Automatic Test Equipment for Analog to Digital Converter Linearity Testing

Darwin C. Mangca[1]
[1]College of Engineering and Information Technology, Surigao State College of Technology, Surigao City, Surigao Del Norte, Philippines-8400

Abstract**—***This paper presents a new approach to testing the linearity of analog to digital converters (ADC) by using field-programmable gate arrays (FGPA) and low-end automatic test equipment (ATE). The higher the ADC resolution, the higher the requirement for ATE. Low-end ATEs have a noisy ramp compared to high-end which is not very useful in linearity testing of ADCs but with the use of FPGA programmed to detect and remove noise, this problem can be solved. The experimental results showed that the FGPA can be used to detect and remove noise. With this, low-end ATEs can be used for ADC linearity testing.*

Keywords**—** *machine noise detection, automated test equipment, FPGA*

I. INTRODUCTION

The necessity for high-end electronic products has increased considerably in recent years due to the ever-competitive electronics industry. As the physical sizes of cell phones, video players, laptops, and digital cameras get smaller, so must the electronic chips that operate them. This will remain a constant challenge in the field.

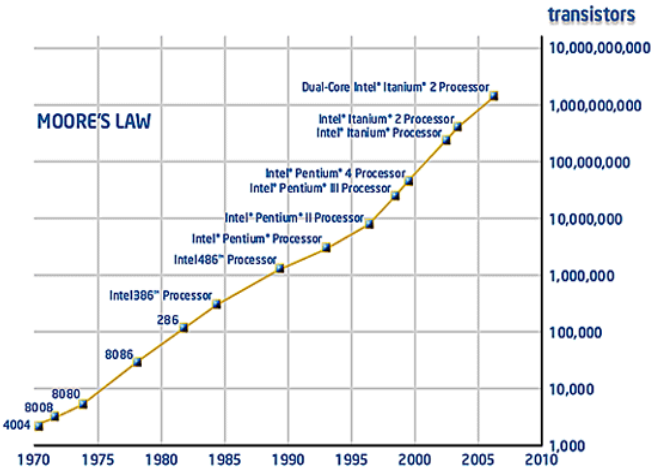

Fig. 1.Moore's Law.

In recent times, this task has been made possible due to the advancement of fabrication methods that enable more transistors to be integrated into a single electronic chip. This is the trend as described by Moore's Law as shown in Figure 1; "the number of transistors on integrated circuits doubles approximately every two years in the same die area" [1][2][3].

With the growing demand for high-performance mixed-signal applications, designers were motivated to produce high performance, high resolution, and low noise ADC [4]. These devices are used to convert analog signals to digital signals as shown in Figure 2 [5][6][7]. Popular usage of ADC is in computers, cell phones, microcontrollers, digital signal processing, digital storage oscilloscopes, scientific instruments, music reproduction, automotive [8].

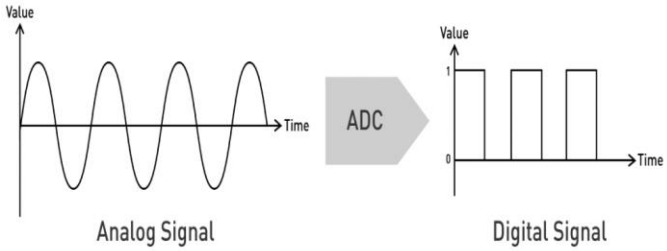

Fig. 2. Analog to Digital Converter (ADC).

The resolution is a very important factor in determining the smallest analog signal that can be converted using ADCs The higher the resolution, the higher the number of binary representations which increases the accuracy of the signal being processed [9][10][11][12]. In the music industry, high-resolution ADCs are needed to convert from audio signals to digital signals accurately which are then uploaded to online video platforms such as youtube or converted to a digital file MP3 or MP4.

This audio is then reconstructed using digital to analog converters (DAC). Audio enhancements can be done after the conversion of data to digital [13][14][15]. Some of these audio enhancements are noise removal, tune correction, time or speed correction, etc.

High-resolution ADCs have a very high requirement for ATEs which makes them more expensive [16][17]. Big chip industries perform several operational tests on the chips before they get sold to the market to ensure that it performs well and are durable within their specifications to avoid losing customers' trust and improve the company's reputation.

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Customer trust is a must need for companies to generate more income.

Linearity testing is one of the parameters that needed to be tested and is quite important because this will identify the ADCs' performance [18][19][20][21]. The higher the resolution of the ADCs, the higher ramp specifications it requires.

Normally, performing a linearity test requires a ramp that can handle several hits per code [22][23][24]. The higher the number of hits per code, the lesser the angle of inclination. A sample ideal ramp test on ADC is shown in Figure 3. A low-end ATE produces a noisy ramp which affects the testing of linearity compared to a high-end ATE. Of course, a high-end ATE is much more expensive compared to a low-end ATE.

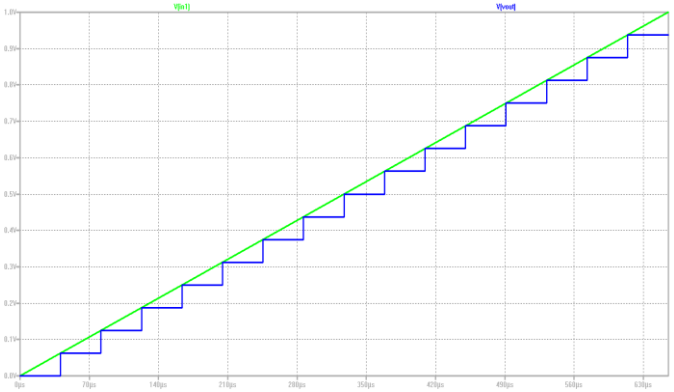


Fig. 3. Ideal RAMP test on ADC.

Before feeding the ADC output to the linearity computing module of the FPGA, a spike noise detection and removal can be done to remove all those unwanted noises. This paper will focus only on noise detection and removal as a solution to used low-end ATEs resulting in increasing the company savings which is very helpful for start-up companies with limited budgets for testing.

II. FPGA Background

Field programmable gate arrays (FPGA) are semiconductor devices that have programmable interconnects around the configurable logic blocks (CLBs) that are in matrix form [26][27]28][29][30]. These can be programmed to different algorithms unlike the application-specific integrated circuits (ASIC). The advantage of FPGA is that it can be reprogrammed anytime based on the needs of the client.

With their reprogrammable nature, FPGAs are very popular in a very wide market such as aerospace & defense, ASIC prototyping, automotive, broadcast and pro AV, consumer electronics, data center, high-performance computing and data storage, etc.

In the production area, if a process can be automated, then it can lessen the production cost. Before FPGAs were available, engineers took time on automating processes. This is because when designing an automation process, the designer needs to convert the program into a custom circuit implementation. Issues involved in creating a custom circuit implementation are the fabrication cost and the time to translate the algorithm into hardware. Implementation of an algorithm with 1000+ lines of the custom circuit would consume a lot of time. With an FPGA, the cost of the chip is a lot less costly since these are mass-produced and translating an algorithm to a custom circuit is a lot faster.

III. Design of Machine Noise Detection and Filtering

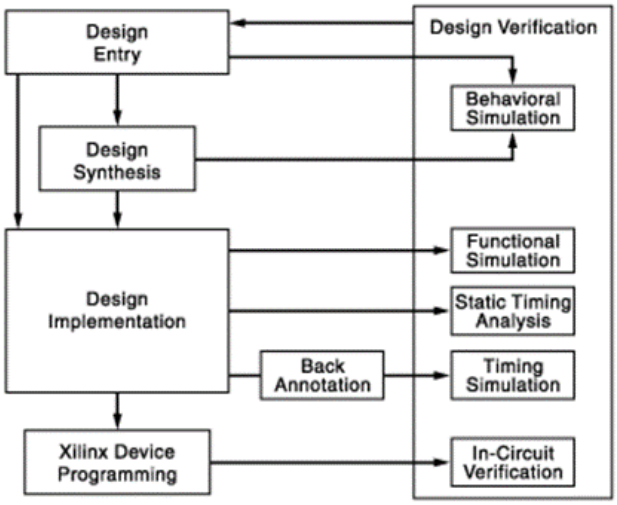


Fig. 4. Design Flow Chart

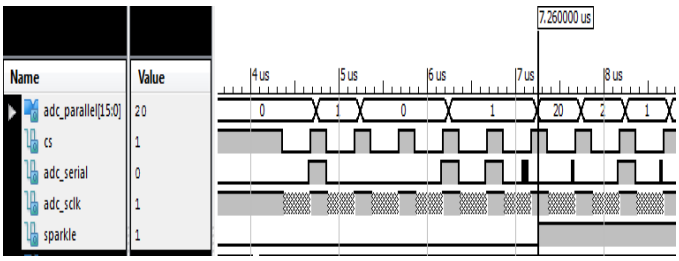
As shown in Figure 4, the design entry was the start of the process. Design entry consists of creating the specifications, designing the algorithm, and converting the algorithm to RTL coding. In this project, the register-transfer level (RTL) language is used as Verilog.

Verilog is a hardware description language (HDL) that is popular in designing and verification of digital circuits. Design Entry was synthesized and has undergone behavioral simulation to verify the design specifications.

Design Synthesis is the process of converting the RTL code into a netlist (list of nets) connecting gates or flip flops. After design synthesis, the design was implemented after meeting the desired design specifications.

In the design implementation, the researcher verified the Functional Simulation and checked the Static Timing Analysis and Timing Simulation. Design Implementation was the process where the netlist was physically placed and mapped to FPGA physical resources. Lastly, a file that can be uploaded on the FPGA was produced during this process.

IV. Results



(a)

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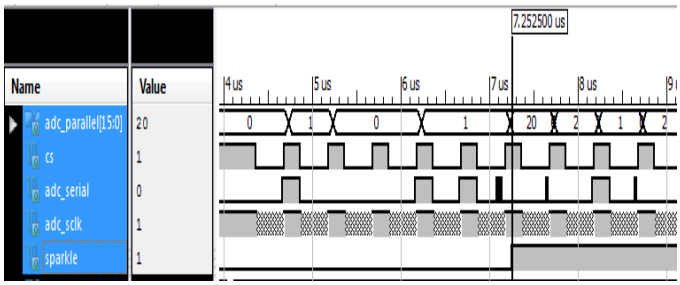

(b)

Fig. 5. Figure 8. Machine noise detection and filtering: (a) Behavioral, (b)Post-Route Simulation

Sparkle Codes or machine noises were unwanted spikes produced by the ATE and are normally found on the low-end type. These errors are produced by the ATE and not from the ADCs that are under test and these will affect the linearity performance.

For this test, a sparkle code "20" was inputted into the system as shown in Figure 5 where the input sequence was 1, 0, 0, 1, 1, **20**, 2, and 1. Simulation results showed that sparkle was detected and after detection, it will be filtered.

TABLE I. Sample Input Sequence for Sparkle Code Detection and Filtering

Sequence	Sparkle Code Detected	Filtered
2,2,3,2,**25**,2,2,3,2	TRUE	TRUE
5,5,6,4,5,**35**,5,4,6	TRUE	TRUE
25, 25, 26, **44**, 24, 25, 25, 24, 26	TRUE	TRUE
53, 55, 55, 54, **70**, 55, 55, 54, 53	TRUE	TRUE
253, 255, 255, **555**, 254, 255, 255, 254, 253	TRUE	TRUE
-307, -309, -308, -306, -307, -308, -309, **-400**, -308	TRUE	TRUE
-632, -633, -635, -633, -634, -635, -633, **-855**, -633	TRUE	TRUE
-855, -855, -855, **-940**, -855, -856, -855, -855	TRUE	TRUE
-944, -945, -944, -945, -944, -944, **-1056**, -945, -945	TRUE	TRUE
-1022, -1023, -1022, -1023, **-1159**, -1022, -1022, -1022, -1022	TRUE	TRUE

Several sequences were also inputted for sparkle code detection and filtering to ensure that the FPGA runs smoothly for both behavioral and post route simulation with no timing errors as shown in Table I. Experimental results showed that there were no errors found during the simulation.

V. Conclusions

A design implementation of the machine noise detection and filtering using FPGA was successfully implemented using Verilog code. The behavioral and post-route simulation was applied to verify the full functionality of the system. The system was able to detect and filter random machine noise or sparkle codes. Also, there were no timing issues found during the verification.

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References

[1] Schaller, Robert R. "Moore's law: past, present and future." IEEE spectrum 34.6 (1997): 52-59.
[2] Mollick, Ethan. "Establishing Moore's law." IEEE Annals of the History of Computing 28.3 (2006): 62-75.
[3] Brock, David C., and Gordon E. Moore, eds. Understanding Moore's law: four decades of innovation. Chemical Heritage Foundation, 2006.
[4] Mangca, Darwin C., et al. "On-the-fly computation method in field-programmable gate array for analog-to-digital converter linearity testing." Journal of Engineering and Technological Sciences (2018).
[5] Rauth, David A., and Vincent T. Randal. "Analog-to-digital conversion. part 5." IEEE instrumentation & measurement magazine 8.4 (2005): 44-54.
[6] Ambardar, Ashok. Analog and digital signal processing. BOSTON, MA: PWS, 1995.
[7] Kosonocky, Stephen, and Peter Xiao. "Analog-to-digital conversion architectures." Digital Signal Processing Handbook (1999): 106-119.
[8] van Veldhoven, Robert, et al. "9.8 A Low-Cost 4-Channel Reconfigurable Audio Interface for Car Entertainment Systems." 2020 IEEE International Solid-State Circuits Conference-(ISSCC). IEEE, 2020.
[9] Bai, Qing, Amine Mezghani, and Josef A. Nossek. "On the optimization of ADC resolution in multi-antenna systems." ISWCS 2013; The Tenth International Symposium on Wireless Communication Systems. VDE, 2013.
[10] Fan, Hua, and Franco Maloberti. "High-resolution SAR ADC with enhanced linearity." IEEE Transactions on Circuits and Systems II: Express Briefs 64.10 (2016): 1142-1146.
[11] Sarhang-Nejad, Mohammad, and Gabor C. Temes. "A high-resolution multibit Sigma Delta ADC with digital correction and relaxed amplifier requirements." IEEE Journal of Solid-State Circuits 28.6 (1993): 648-660.
[12] Jansson, Christer. "A high-resolution, compact, and low-power ADC suitable for array implementation in standard CMOS." IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications 42.11 (1995): 904-912.
[13] Zölzer, Udo. Digital audio signal processing. John Wiley & Sons, 2008.
[14] Spanias, Andreas, Ted Painter, and Venkatraman Atti. Audio signal processing and coding. John Wiley & Sons, 2006.
[15] Rao, Preeti. "Audio signal processing." Speech, Audio, Image and Biomedical Signal Processing using Neural Networks. Springer, Berlin, Heidelberg, 2008. 169-189.
[16] Pellati, Paolo, and Piero Olivo. "Automated test equipment for research on nonvolatile memories." IEEE Transactions on Instrumentation and Measurement 50.5 (2001): 1162-1166.
[17] Kuenzi, Creston D., and Christopher D. Ziomek. "Fundamentals of oscilloscope measurements in Automated Test Equipment (ATE)." 2006 IEEE Autotestcon. IEEE, 2006.
[18] Yu, Zhongjun, and Degang Chen. "Algorithm for dramatically improved efficiency in ADC linearity test." 2012 IEEE International Test Conference. IEEE, 2012.
[19] Chen, Tao, et al. "A low-cost on-chip built-in self-test solution for ADC linearity test." IEEE Transactions on Instrumentation and Measurement 69.6 (2019): 3516-3526.
[20] Uemori, Satoshi, et al. "ADC linearity test signal generation algorithm." 2010 IEEE Asia Pacific Conference on Circuits and Systems. IEEE, 2010.
[21] Kuyel, Turker. "Linearity testing issues of analog to digital converters." International Test Conference 1999. Proceedings (IEEE Cat. No. 99CH37034). IEEE, 1999.
[22] Max, Solomon. "Ramp testing of ADC transition levels using finite resolution ramps." Proceedings International Test Conference 2001 (Cat. No. 01CH37260). IEEE, 2001.

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[23] Jiang, Wei, and Vishwani D. Agrawal. "A DSP-based ramp test for on-chip high-resolution ADC." 2011 IEEE 43rd Southeastern Symposium on System Theory. IEEE, 2011.
[24] Wen, Yun-Che, and Kuen-Jong Lee. "An on chip ADC test structure." Proceedings of the conference on Design, automation and test in Europe. 2000.
[25] Rose, Jonathan, Abbas El Gamal, and Alberto Sangiovanni-Vincentelli. "Architecture of field-programmable gate arrays." Proceedings of the IEEE 81.7 (1993): 1013-1029.
[26] Rose, Jonathan, Abbas El Gamal, and Alberto Sangiovanni-Vincentelli. "Architecture of field-programmable gate arrays." Proceedings of the IEEE 81.7 (1993): 1013-1029.
[27] Brown, Stephen D., et al. Field-programmable gate arrays. Vol. 180. Springer Science & Business Media, 1992.
[28] Meyer-Baese, Uwe, and U. Meyer-Baese. Digital signal processing with field programmable gate arrays. Vol. 65. Berlin: springer, 2007.
[29] Rose, Jonathan, et al. "Architecture of field-programmable gate arrays: The effect of logic block functionality on area efficiency." IEEE Journal of Solid-State Circuits 25.5 (1990): 1217-1225.
[30] Rose, Jonathan, et al. "Architecture of field-programmable gate arrays: The effect of logic block functionality on area efficiency." IEEE Journal of Solid-State Circuits 25.5 (1990): 1217-1225.

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