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Printed SMT Design for Alternative Packaging Technology

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I. Overview

- The direction for thinner and densified version of Quad Flat No-lead (QFN) device benefits thermal performance and increased in number of I/O respectively.
- QFN is one form of Surface Mount Technology (SMT) composed of a silicon die bonded to a lead through wire.
- The overall unit is encapsulated by a molding compound material to protect the active circuit of the unit.

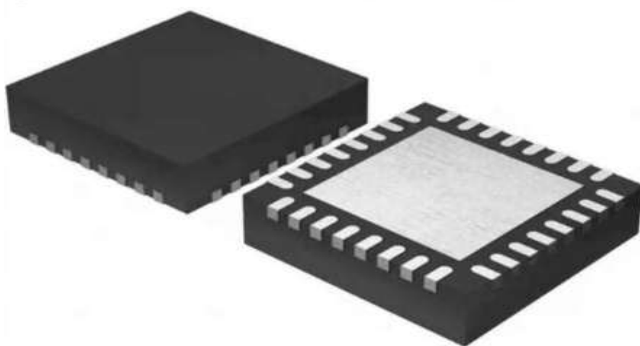

Fig. 1. QFN

- Standard body size of QFN has a typical number of I/O count ranges from 20-40.
- The difference of this package to other form of SMT is the absence of pin to attach the unit in the PCB boards.

II. Problem Identification

- Continuous development to widen/broaden the current capability of QFN is the interest of semiconductor companies.
- There are multiple packaging technologies like Thin Quad Flat No-lead (TQFN) or Ultrathin Quad Flat No-lead which offers thinner version of QFN devices in semiconductor industry.
- Due to fabrication limitations, either design or material related, I/O count is limited to a minimum number.
- A thinner packaging with capability of higher number of I/O count is the interest of semiconductor companies for the future of QFN technology.

III. Design Solution and Improvement

- The innovative packaging technique covers new SMT design and method of fabrication wherein the silicon die and wirebond material is directly attach to the thin layer of printed conductive material.
- The overall unit is encapsulated by molding where the printed conductive material is left exposed to the bottom.
- The printed conductive material provides connection to the PCB.

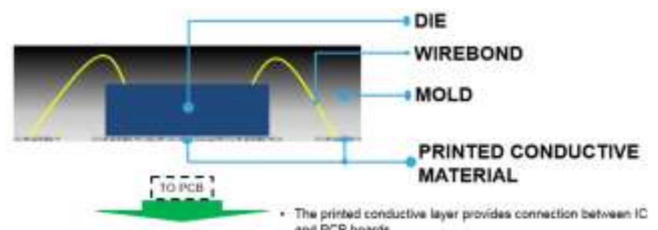

Fig. 2. Printed SMT design

- Printing of conductive material to the carrier can be through stencil process or similar processes.
- Dual or multiple arrays of I/O can be printed for interconnection.
- The carrier where the conductive material will be attach can be through stainless alloy wherein it can easily detach upon encapsulation of unit.

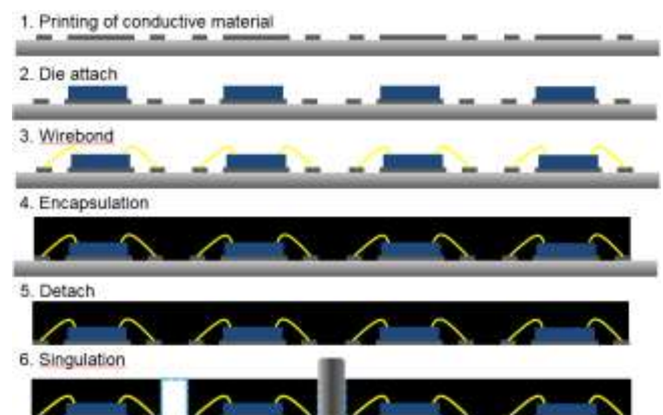

Fig. 3. Method of fabrication

- Through incorporating a printed conductive layer instead of leads and thermal pads the package thickness can be reduced by 30-40% from the conventional architecture.