Substrate Design Augmentation to Address Wire to Solder Mask Shorting

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I. OVERVIEW

Recently, new technologies in semiconductor electronics industry are getting augmented and one of the challenges is the design of the material to be used. The product in focus on this paper is one of the major products in the market as it used on wide range of applications such as smartphones, security devices and automated teller machine (ATM) cards. Fig.1 shows the assembly manufacturing process flow of the product with the wirebonding process as the most challenging task.

Fig. 1. Assembly process flow.

II. PROBLEM IDENTIFICATION

During the development phase of the product, one of the top assembly rejects is the wire touching or shorting with the solder mask as highlighted in Fig. 2. This is mainly because of the lead finger or bond finger submerged or under the cavity with respect to the top surface of the solder mask. More importantly, the reject is manifested during wirebonding process.
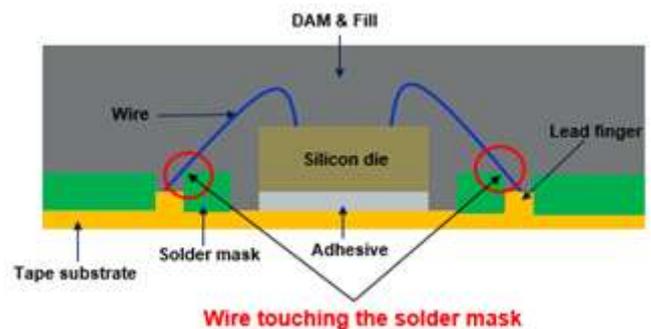

Fig. 2. Occurrence of wire shorting.

This reject manifestation will eventually fail during the reliability of the product. By the growing demand in the market for this product, indeed this is a very big challenge especially during the package development phase.

III. SEMICONDUCTOR PACKAGE DESIGN SOLUTION

An augmented and improved semiconductor substrate design is presented in Fig. 3 wherein the bond finger or lead finger is coplanar or leveled with the solder mask surface.
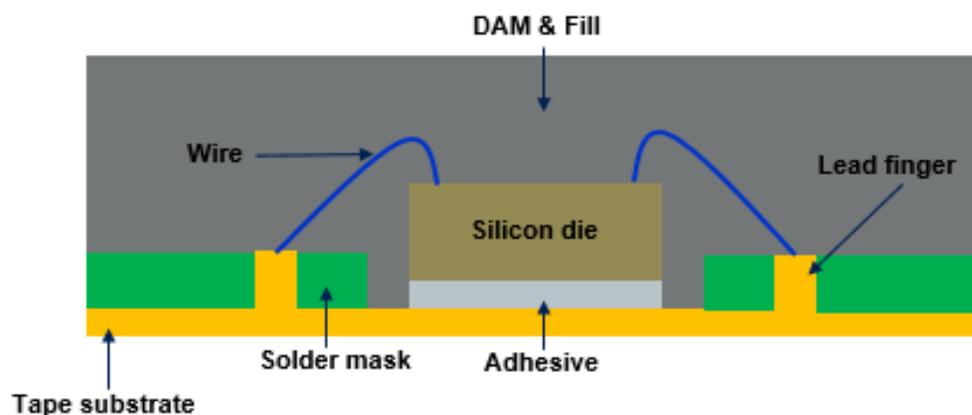

Fig. 3. Substrate design augmentation.

The improved substrate design will eliminate the occurrence of the top assembly reject during the assembly manufacturing of the product. Furthermore, the design will also result to better reliability of the product.