

# Insights into the Thermal Management Performance of QFN Package with Embossed Die Pad

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Abstract— Power devices in QFN platform requires efficient thermal management system. The use of conductive glue, sintered or semisintered adhesives, or solder materials ensure effective thermal dissipation. Herein, a new leadframe design where embossed patterns are introduced into the die pad is evaluated. Insights into the effect of the introduced design feature in terms of thermal dissipation are discussed. In brief, the embossed pattern results in minimal thermal gain of about 1 % using power glue, and about 3% using a 30 µm conductive die attach film (cDAF). Reducing the cDAF thickness is expected to further increase the thermal gain.

Keywords— Embossed, matrix, power glue, thermal dissipation, cDAF.

#### I. INTRODUCTION

The growing demand in portable wireless technologies is driving the development of more functionality, faster performance and smaller footprint electronic packages. The QFN (Quad Flat No-Lead) package has been developed for portable wireless electronic devices. It does not have the outer leads to reduce the mounting space. The board-level interconnections are peripheral flat terminals at the bottom of the package. The advantages of this advanced package are miniaturized footprint, good thermal performance and excellent electrical characteristics. The thermal performance of the electrical package can be improved by reducing the thermal resistance between the package and the board, which resulting in dissipating heat efficiently into the printed circuit board, and enhancing the package effective area to increase air convection. Due to the short thermal path of the package, the thermal resistance between QFN package and board is smaller, so the package has good thermal performance.

However, for power applications, there is an inherent limitation for this package type. This is due primarily to its relatively thin leadframe and epoxy die attach (DA) material. The QFN package was used as a starting point to develop an improved power IC package. The power package combines the attributes of older and larger HSOP power packages with the surface efficiency of the newer QFN package. Power Quad Flat No-lead (PQFN) is a surface mount plastic package with lead pads located on the bottom surface of the package. All PQFN packages have either been designed with a single exposed die pad or multiple exposed die pads depending on device requirements and intended application. The small footprint provides a cost effective and area efficient solution for multi-chip power IC products. The PQFN uses the same basic manufacturing scheme and construction as the QFN. As a result, the comparative cost of the PQFN is less than that of the existing HSOP industry standard power IC package.

### II. DESIGN AND PROCESS SOLUTION

Existing package design for QFN (Fig. 1) consists of flat surface pad (1), conductive die attach films (2), die (3) with backside metallization (4) connected through vias (5) to the active metallization of the die. To have an electrical continuity within the package construction, most package have backside metallization connected to the active part of the die. (4) will have an interface with (2) to attach (3) with (1). To gain electrical and thermal continuity, metal fillers occupies most of the (2) material formulation. In particular, silver is the most adapted for die attach film application due to its good electrical and thermal conductance.

Higher silver content of (2) results in lower thermal and electrical resistivity. The primary limitation on the achievable thermal and electrical conductivity enhancement effected by the silver formulation on die attach film as compared with die attach glue is the allowable amount of silver content in the formulation. Electrical and thermal conductivities are determined by the distance of the die to the surface of the pad (2), the contact area between the interfaces, and the material compositions for the package.

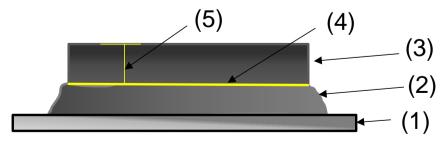


Fig. 1. Cross-sectional illustration of a standard leadframe-based device.

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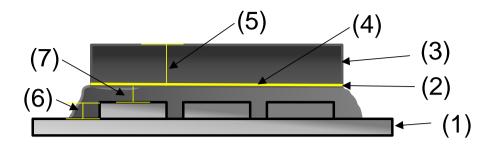
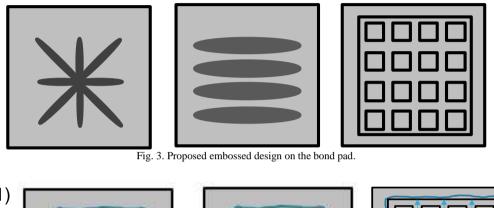


Fig. 2. Cross-sectional illustration of a leadframe-based device with embossed pad.



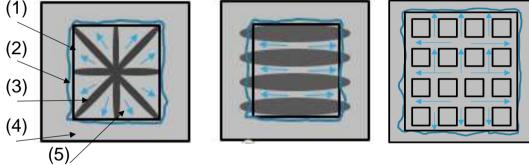


Fig. 4. Proposed embossed design showing air and DAF squeezed out pathway. 1-die, 2-DAF squeeze out, 3-embossed Pattern, 4-pad, 5-space for DAF squeeze.

By decreasing the distance of the backside metallization to the pad and increasing the interfacial contact area result in lower electrical and thermal resistivity within the package construction. The addition of embossed metal (Fig. 2) with variable height (6) on the pad design will decrease the distance between (4) and (1), *i.e.* (7), without altering DAF height (6 + 7) requirement of the package is expected to promote better thermal dissipation and electrical conduction. Depending on the design of the embossed metal, the contact area of (pad-to-DAF) interface increases providing improved interfacial transport of heat and current. It follows that by optimizing the design of the leadframe through the introduction of embossed metal on the pad (Fig. 3), enhanced thermal dissipation and electrical conductivity is achieved within the construction of the package realizing the possibility of producing packages with high thermal and electrical conductivity requirements.

Based on preliminary die bond simulation, there are pathways for air and DAF squeezed out during bonding (Fig. 4). These reduce the risk of voids due to the introduction of embossed metal layer at pad ensuring manufacturability.

The improved leadframe design still meets the required DAF height requirement of the package. The importance of maintaining the thickness of the DAF is to render cushioning effect during thermal and dynamic differences along the package construction.

Thermal analysis via simulation using the system with embossed die pad (square grid matrix) was performed to assess the applicability of the proposed solution. Using a power glue with a thermal conductivity of 6 Wm<sup>-1</sup>K<sup>-1</sup> and a BLT of 30  $\mu$ m in a QFN 6 x 6 x 1 mm package, with pad size of 4.1 x 4.1 mm<sup>2</sup>, frame thickness of 200  $\mu$ m, and die dimensions of 3 x 3 x 0.28 mm results in a thermal gain of around 1 %. Increasing the pad pitch from 100 to 640  $\mu$ m did not result in a significant thermal gain. However, using the same system but with a conductive die attach film with thickness of 30  $\mu$ m results in a 3% thermal gain. It is expected that by decreasing the thickness of the DAF, the thermal gain can be further improved due to the further reduction of the die-



to-die pad distance.

It is worth noting that the introduction of the embossed pad matrix will introduce further contact resistances between the different layers and materials involved. This could possibly lead to a worsening in terms of  $RTH_{J-A}$  which cannot be previewed by thermal simulations. Further evaluations are recommended.

## III. CONCLUSION

Providing new leadframe designs with embossed die pad offered an innovative solution to enhance the high thermal and electrical conductivity of QFN packages. In effect, the embossed pad design leads to thermal gain by reducing the die-to-die pad distance, ensuring shorter thermal and electrical dissipation pathways. Additional thermal simulations and process validations are recommended to optimize the usability and workability of the proposed solution.

#### REFERENCES

 C.-L. Chang, Y.-Y. Hsieh, "Thermal analysis of QFN packages using finite element method," 5<sup>th</sup> International Conference on Thermal and Mechanical Simulation and Experiments in Microelectronics and *Microsystems*, 2004. EuroSimE 2004. Proceedings of the, Brussels, Belgium, 2004, 499-503.

- [2] A.C. Lu, et al, "Electrical and Thermal Modelling of QFN Packages," IEEE Electronic Packaging Technology Conference, 2000, 352-356.
- [3] C. C. Ng, "Thermal performance evaluation of Power QFN package with stacked and side by side die configuration," 2015 10<sup>th</sup> International Microsystems, Packaging, Assembly and Circuits Technology Conference (IMPACT), Taipei, 2015, 184-187.
- [4] M. Nachnani, P. Rogren and Y. Sun, "Configurable sintered interconnect (CSI) DAP-less QFN package for high thermal performance application," 2015 IEEE 17th Electronics Packaging and Technology Conference (EPTC), Singapore, 2015, 1-6.
- [5] F. Poh KS, Tan Hien Boon, Krishnamoorthi Sivalingam, Lim Beng Kuan, A. Y. S. Sun and Rahamat Bidin, "Development of high power QFN package," *IEEE/CPMT/SEMI 29<sup>th</sup> International Electronics Manufacturing Technology Symposium*, San Jose, CA, USA, 2004, 295-300.
- [6] Y. Y. Ma, S. Krishnamoorthi, C. K. Wang, A. Y. S. Sun, W. H. Zhu and H. B. Tan, "On the thermal characterization of an exposed top quad flat no-lead package," 2006 8<sup>th</sup> Electronics Packaging Technology Conference, Singapore, 2006, 810-814.
- [7] S. Krishnamoorthi, K. Y. Goh, D. Y. R. Chong, R. Kapoor and A. Y. S. Sun, "Thermal characterization of a thermally enhanced QFN package," *Proceedings of the 5<sup>th</sup> Electronics Packaging Technology Conference* (EPTC 2003), Singapore, 2003, 485-490.