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Realization of Wettable Sidewall for Quad Flat No-Lead Devices

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***Abstract*—** *Incorporating a wettable sidewall in quad flat no-lead devices is one the new requirement of automotive customers to improve its performance in board level application. An alternative solution is through leadframe design modification in conjunction with optimizing the singulation and the plating processes to create a quad flat no-lead (QFN) device exhibiting good wettability at the lead sidewall.*

***Keywords*—** *Silicon die; Semiconductor Die; Wettable flank; Design Improvements*.

I. INTRODUCTION

The expansion of integrated circuit in automotive application implies additional requirement for the packaging technique of conventional surface mount technology (SMT) devices to incorporate "*wettable sidewalls*" on the lead configuration to improve solder wettability in the lead junction. Moreover, the solder wetting developed at the lead junction is used as a visual reference for good Sn distribution underneath the integrated circuit device. Due to the method of assembly for QFN or other leadframe-based products (Fig. 1), a mechanical blade is generally used as a means of separating each individual component resulting in exposed copper material at the sidewall of the conventional IC. The copper material is known to be unstable in nature and easily forms chemical bonds in oxygen from the atmosphere resulting in the formation of copper oxides as the by-product of the copper - oxygen interaction. The copper oxide at the lead junction has the property of poor solderability for the solder material.

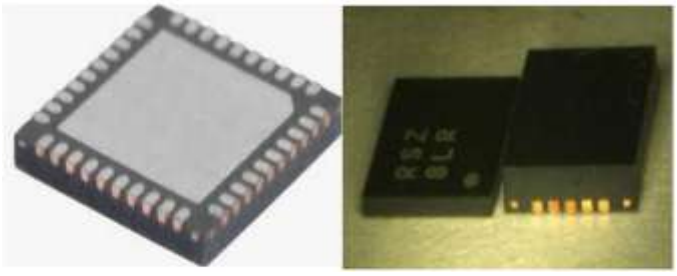

Fig 1. Conventional QFN Package

Herein, a novel design and fabrication method for QFN to produce a "*wettable sidewall*" is discussed and presented. The solution provides an essential alternative in the qualification of QFN and leadframe-based devices for automotive application (Fig. 2).

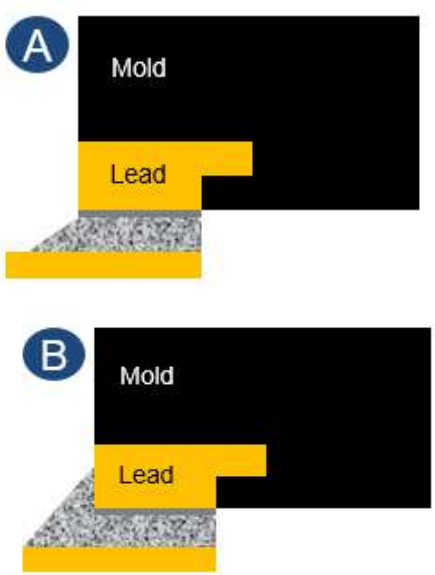

Fig 2. (A) Conventional QFN, (B) Automotive requirement with visually detectable solder joint through wettable flank.

II. RELATED LITERATURE

Plating is a technique used in surface covering wherein a metal is deposited on the outer conductive surface. This method has been practiced and adapted in the past and still vital in modern application and technology. In the semiconductor industry, plating is widely recognized as an adhesion and wettability promoter for leadframe-based devices and an alternative option for corrosion and oxidation prevention/elimination for other surface mount devices such as substrate and ceramic based devices. Moreover, plating became known in board level assembly also as solderability and wettability enhancer between the PCB and integrated circuit device.

III. PROCESS AND PACKAGE DESIGN SOLUTION AND IMPROVEMENT

Producing a plated sidewall in the lead area is one of the alternative and potential solution in producing a "*wettable sidewall*" for conventional QFN. Through modification in the current process flow and leadframe configuration, the proposal can be realized.

In Fig. 3, a cross sectional illustration of the proposal is indicated wherein the lead junction is fabricated with sidewall plating. In Fig. 4, the method of fabricating a wettable sidewall on the leadframe is explained. Fig. 4A shows an illustration of a bare leadframe. Afterwards, an etching

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process is done to produce a half-etch area in the leadframe, as shown in Fig. 4B. The half-etch and bottom part of the leadframe will be plated as shown in Fig. 4C, with a defined thickness of conductive material such as Sn, flashes of gold or silver to cover the outer surface of the leadfame.

Fig. 5 outlines the method of exposing the plated sidewall through a mechanical blade. A defined thickness of the plating at the sidewall with correct combination of mechanical blade tolerance can be maximized to achieve correct thickness of the plating layer.

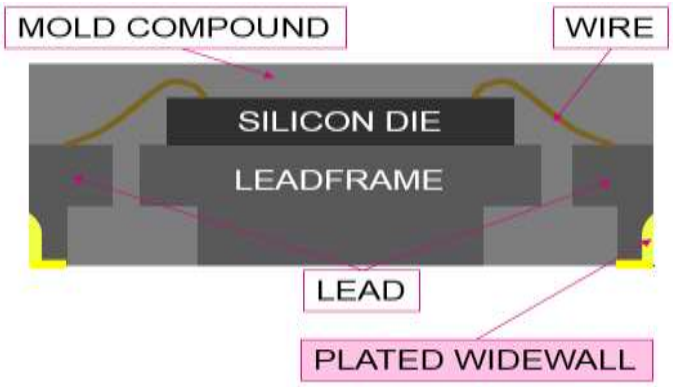

Fig. 3. Illustration of the proposal

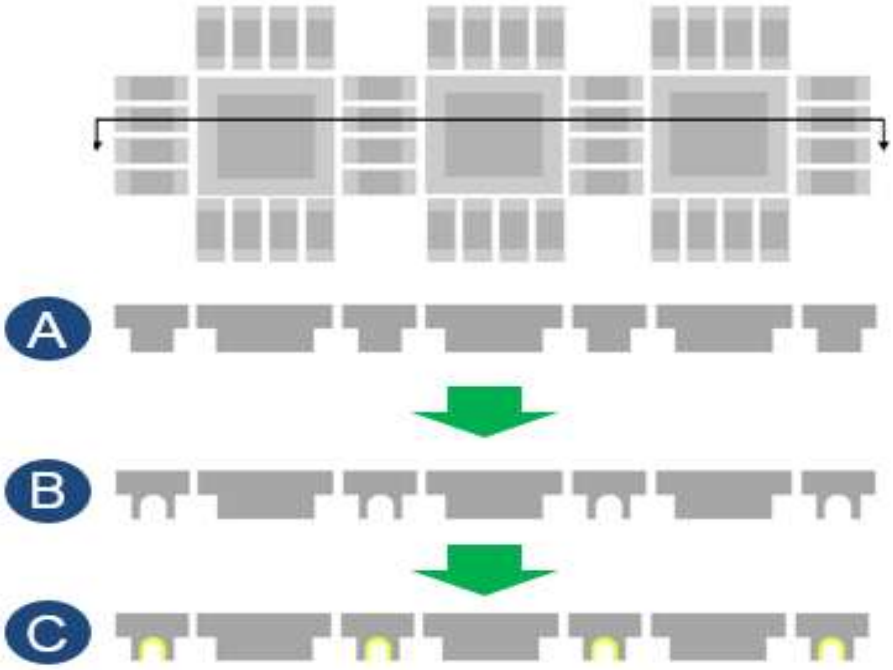

Fig. 4. Method of leadframe fabrication for the proposal.

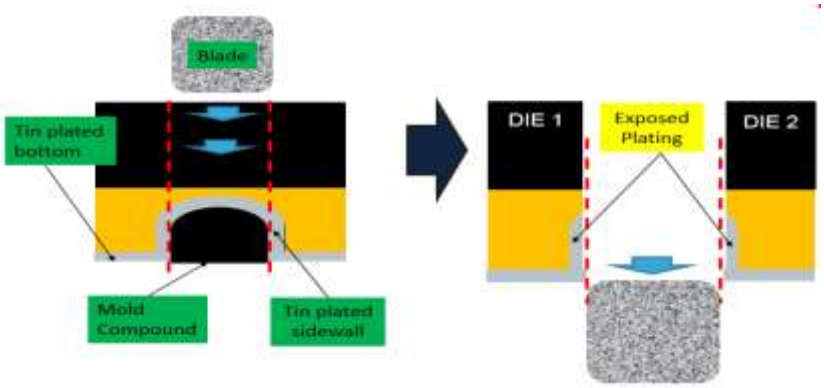

Fig. 5. Process of singulation

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IV. CONCLUSION

The proposed solution offers a viable alternative over existing methods like partial cut singulation, Sn immersion plating, dimpled leads, etc. with the perceived advantages such as no occurrence of damage units during plating since plating is done prior assembly of IC during leadframe fabrication, and no accumulation of metal burrs since during leadframe fabrication actual process will be chemical etching. However, identified challenges that need to be addressed include plating thickness should be thick enough such that during singulation sufficient Sn plated layer remains, and potential of developing new types of blade compatible to cut tin, leadframe base material (Cu alloy) and epoxy mold compound.

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