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Increasing Chip Functionality in a Limited Package Footprint through Innovative Multiple Die Design and Assembly Process

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Abstract**—** *A semiconductor package containing multiple dies could be assembled using independent assembly flows where each flow involved attaching a die on a carrier or onto another die using a die attach material, and electrically connecting the die to the carrier and/or another die using a wire. The assembled carrier containing two or more dies is mounted onto another assembled carrier containing two or more dies. The assembly containing the carriers, dies, wires and die attach materials are molded using a molding compound. One side of the package can be customized to serve as a footprint for additional die assembly such that another set of one or more die is attached to the package, serving as a carrier, using a die attach material or a bump in the case of chip scale package.*

Keywords**—** *Multiple die, chip scale package, processin power, speed.*

I. INTRODUCTION

Component miniaturization continues to be one of the primary drivers of innovation in the semiconductor and electronics industries [1-2]. Packing millions to billions of transistors in an integrated circuit has defied Moore's Law, with exceptionally advanced technologies such as the next-generation lithography (extreme ultraviolet lithography (EUV-lithography), X-ray lithography, electron beam lithography, focused ion beam lithography, and nanoimprint lithography) enabling the production of 22 nm down to 2 nm technology nodes [3-6]. In the perspective of packaging and assembly manufacturing, miniaturization poses technical challenges by having very limited footprint and highly constrained dimension in all axes. Innovative solutions are necessary to accommodate more functionalities to satisfy stringent requirements on processing speed and power; multi-die packages provide one solution to this technical challenge.

Stacked die separated by layers of spacers or die attach materials qualifies as a physical means associated with enhancing computing capabilities at the device level [7-8]. However, the use of multiple die attach material with different properties makes the interface susceptible to thermomechanical failures [9]. The multiple curing processes tend to weaken adhesion or promote material degradation. In addition, stacked die requires complicated wirebonding profiles, leading to significantly higher wire consumption (Fig. 1).

Herein, an innovative solution to realize multiple die assembly in a very limited footprint is presented. Parallel independent flows lessen repeated die attach process and curing thereby reducing the thermal budget of the device. Innovation in design and assembly process enable multi-die package within and outside the package.

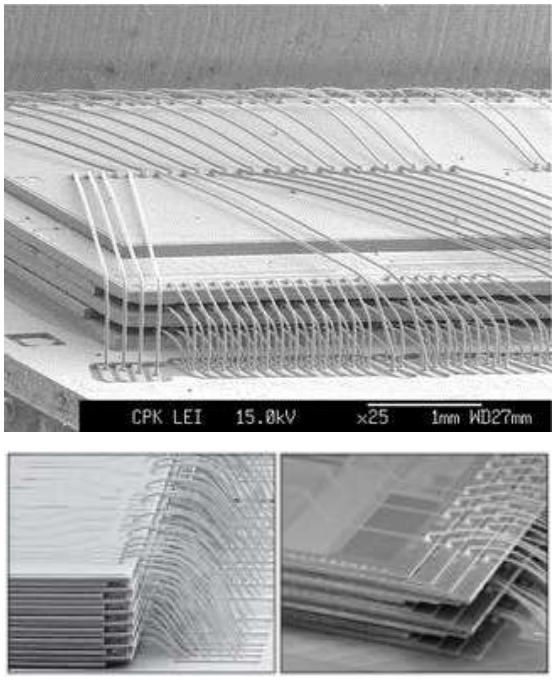

Fig. 1. Chip stack with multiple die attach material and spacers, and complicated wirebonding profiles.

II. DESIGN AND PROCESS SOLUTION

The innovative solution involves multiple independent flow to reduce the overall thermal budget of the device during assembly. Assembly 1 entails the attachment of a die or multiple dies on a carrier using standard die attach processes, and connecting the die with the carrier through wirebonding process. Assembly flow 2 is similar but using a different carrier design. Assembly flow 3integrates the products of the 2 independent assembly flows (Fig. 2 and 3).

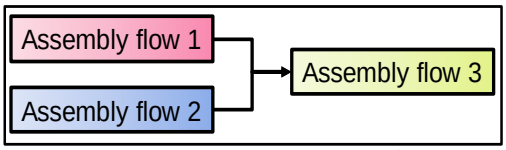

Fig. 2. Multiple independent assembly flows.

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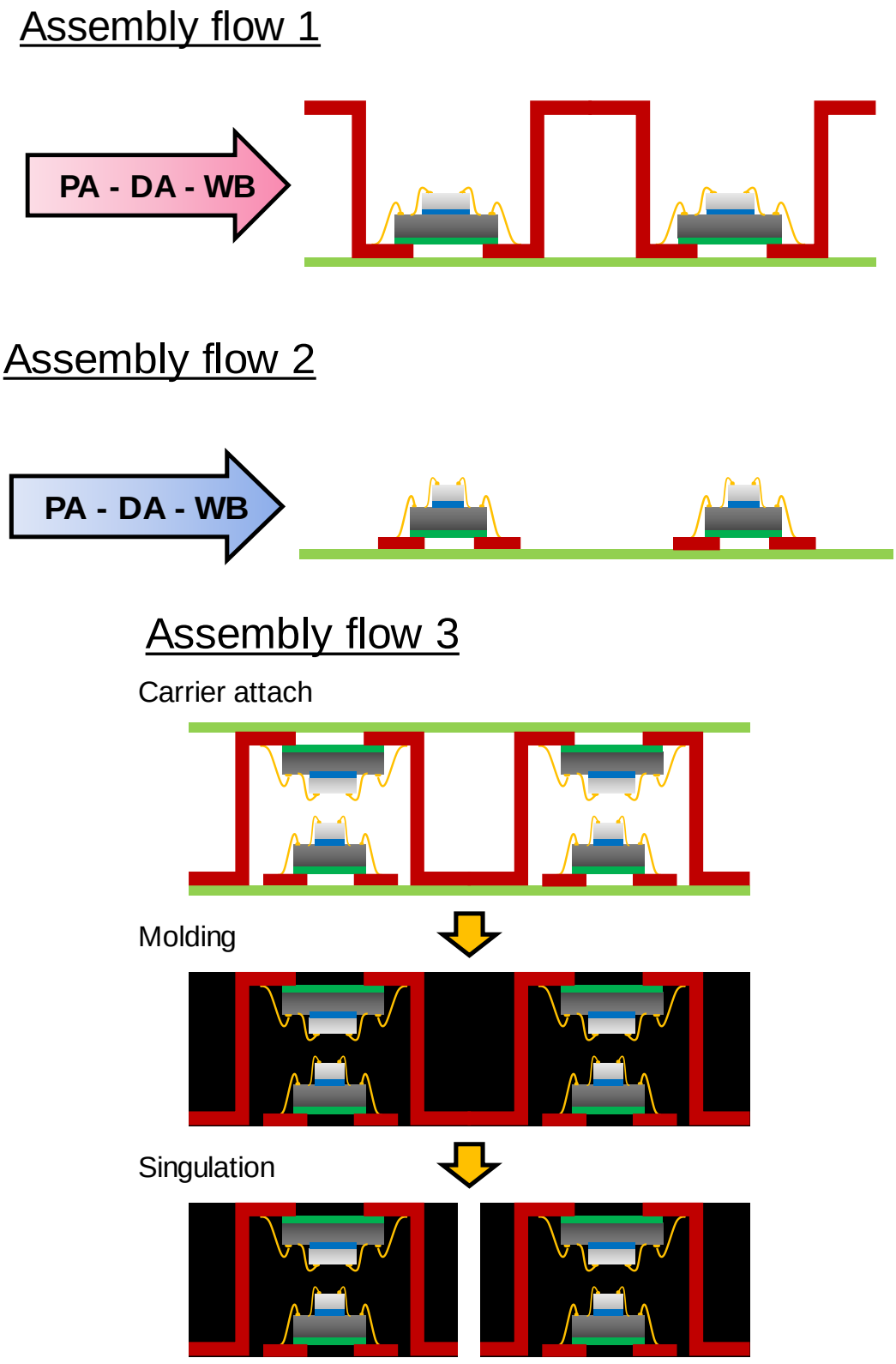

Fig. 3. Assembly flows 1 and 2, and integration (Assembly flow 3) to create the final product. PA – Pre-assembly; DA – die attach; WB – wirebond.

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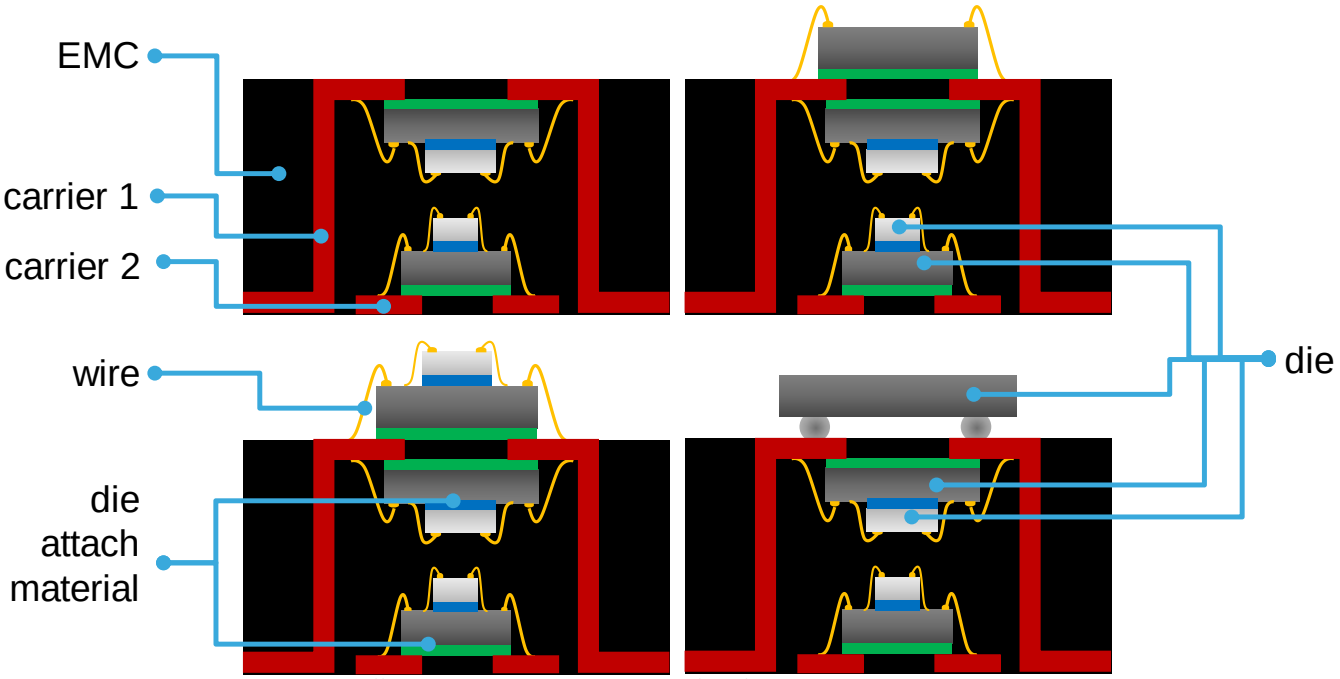

Fig. 4 End product showing different components, and potential platform for outside die stacking. EMC - epoxy mold compound.

After the integration, the built unit could be designed to serve as a carrier for additional die densification. The package top side could serve as a surface for the attachment of a die or a plurality of dies which could be connected through standard wirebonding profiles. In addition, attachment of a chip scale package through the bumps via a reflow process is feasible. This simple customization enables vertical integration at the device packaging level.

III. Conclusion

The novel solution permits the creation of devices containing multiple dies within and outside the device, thus increasing the die density within a given package footprint, resulting in higher processing power or speed. Independent assembly flows to build on carriers 1 and 2 lessen repeated die attach process and curing, and lowers the assembly thermal budget of the entire package. In addition, simpler wirebonding profile and lower wire consumption is expected due to fewer die stack per carrier. The package top side can be customized to serve as footprint for additional die stack.

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