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Integration of Mechanical Interlocking Design on Silicon Die

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Keywords— *Silicon die; Semiconductor Die; Interlocking; Design Improvements.*

I. OVERVIEW

- A silicon die or a die is the core of each integrated devices wherein the functional circuit is fabricated. On a Quad flat-no-grid devices, this silicon die is typically glued to the leadframe pad either by conductive or non-conductive paste depending on the thermal and electrical requirements of the device.

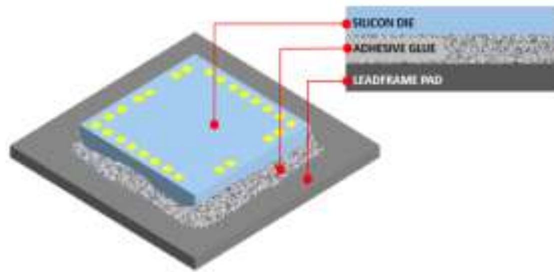

Fig. 1. A 3D view of silicon die that is attached to the leadframe

- In addition, the layer of adhesive material between the silicon and leadframe pad acts as a "cushion" between the materials' different coefficients of thermal expansion (CTE) characteristic.

II. PROBLEM IDENTIFICATION

- A mismatch in the CTE affects integrated circuit devices since it can cause delamination or separation of material between interfaces.

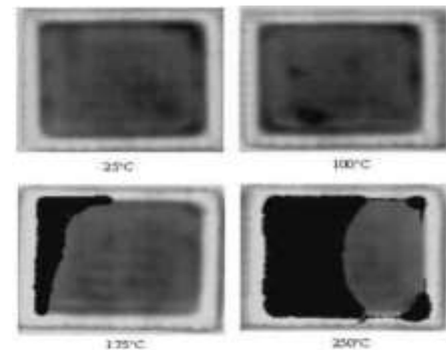

Fig. 2. Sample photo of delamination.

- Fig. 2 shows an example of delamination propagating from the perimeter of the silicon die, slowly peeling the die as temperature increases. The temperature in this case is reliability requirement in QFN devices representing the life of the product in the actual application.

III. PACKAGE DESIGN SOLUTION

- An interlocking mechanism incorporated in the silicon die material increases the interfacial strength of the die and adhesive paste

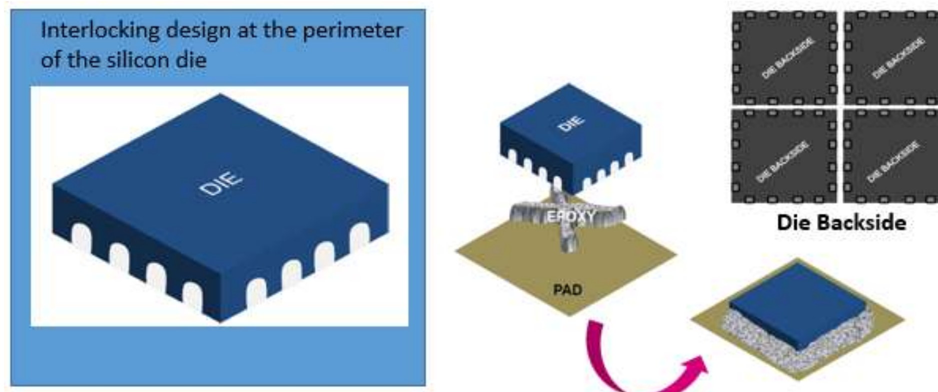

Fig. 3. Illustration of interlocking design on the silicon die.

- The interlocking design can be done through laser or chemical etching process on the backside of the silicon die.