

Semiconductor Die Design with Pre-Applied Die Attach Material

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I. OVERVIEW

- Front-of-line (FOL) processes namely the wafer preassembly and die attach processes have challenges especially in processing thin dice with thickness ranging from 50µm to 120µm
- Typical assembly manufacturing process flow in Fig. 1 shows the mentioned processes at FOL stations



Fig. 1. Assembly manufacturing process flow.

II. PROBLEM IDENTIFICATION

• Potential die-related issues like die cracks, die delamination, and die attach voids in Fig. 2 occur

especially on thin die applications during diebonding or die attach process

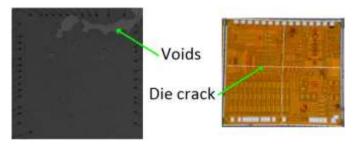
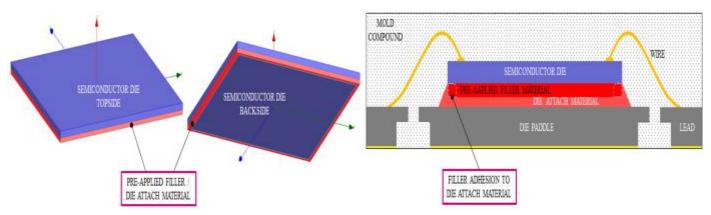


Fig. 2. Die-related anomalies.

• With the increasing demand on thin die applications, mitigation of die-related issues is one big challenge during wafer preparation or pre-assembly and the diebonding process

III. SEMICONDUCTOR DIE DESIGN SOLUTION

- Silicon die backside area is augmented with pre-applied die attach material or filler material on the die's grooved periphery
- With pre-applied filler material, the die attach coverage is enhanced and the die attach adhesion is more robust



The process may follow:

Wafer Taping (Active Side on Tape) \rightarrow Backside Laser Groove \rightarrow Wafer Detaping \rightarrow Filler Mount \rightarrow Curing \rightarrow Wafer Mounting (Backside on Tape) \rightarrow Wafer Sawing

Fig. 3. Semiconductor die augmentation with pre-applied die attach material.

- Laser grooving technology is used for the formation of the peripheral groove
- The semiconductor die design with pre-applied die attach material could help mitigate die to die attach delamination
- Lower coefficient of thermal expansion (CTE) mismatch is created between the pre-applied filler or die attach material and the subsequent die attach material
- With the design, die cracks could be prevented and die attach voids could be minimized

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