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Semiconductor Leadframe Design Augmentation for Thinner and High-Density Package Capability

Rennier S. Rodriguez, Frederick Ray I. Gomez
Central Engineering & Development, Back-End Manufacturing & Technology, STMicroelectronics, Inc.
Calamba City, Laguna, Philippines 4027

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I. BACKGROUND OF THE STUDY

- Semiconductor quad flat no-leads multi-row (QFN-mr) leadframe package offers high density of input/output (I/O) requirement, and utilizes a tapeless leadframe technology that providing mechanical support to the silicon die, wire, and mold during package assembly
- However, as the thickness of the leadframe becomes thinner, the mechanical interlocking to mold compound decreases in terms of the area of contact

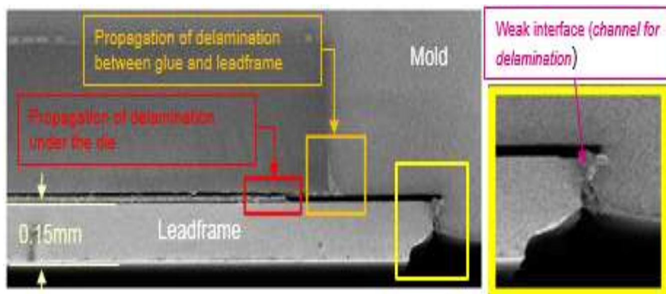

Fig. 1. Cross-sectional illustration of delamination starting from weak interlocking.

- The limitation is associated to the design and manufacturing method of tapeless leadframe

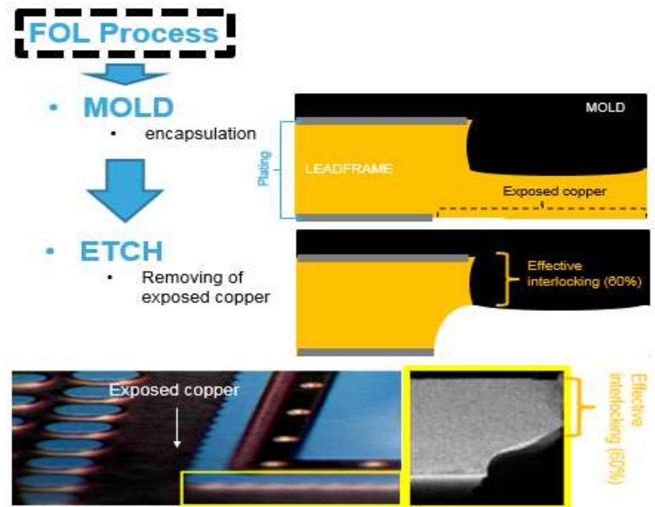

Fig. 2. Illustration of tapeless leadframe process.

- The effective interlocking of tapeless leadframe is only at 60%

II. PACKAGE DESIGN SOLUTION

- A semiconductor QFN leadframe package design augmentation is illustrated in Fig. 3, with the addition of grinding process at the end-of-line (EOL) assembly process

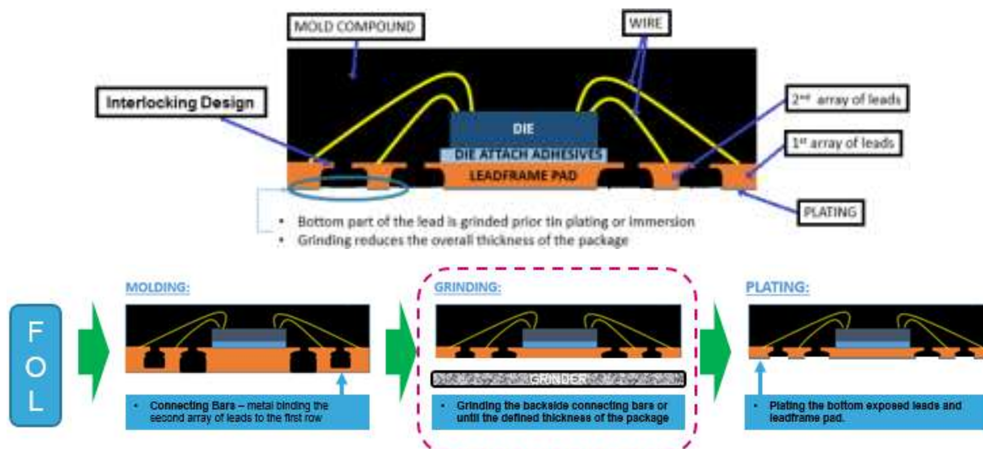

Fig. 3. Semiconductor QFN leadframe design augmentation, showing the process flow for leadframe with connecting bars.

- The improved semiconductor leadframe design covers the QFN miniaturization program with capability of thinner and high-density semiconductor package

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