International Research Journal of Advanced Engineering and Science
ISSN (Online): 2455-9024

Semiconductor IC Package Sidewall Augmentation for Package Chip-out Mitigation

Rennier S. Rodriguez, Frederick Ray I. Gomez
New Product Introduction, Back-End Manufacturing & Technology, STMicroelectronics, Inc.
Calamba City, Laguna, Philippines 4027

Abstract—*The paper presents an improvement on the semiconductor integrated circuit (IC) package's sidewalls for mitigation of package chip-out and for prolonging the singulation blade life.*

Keywords— *Chip-out; sidewall; semiconductor package; blade life.*

I. Background of the Study

- Package chip-out was evident on Device A with measurement greater than the specification (or specs) limit of 125µm

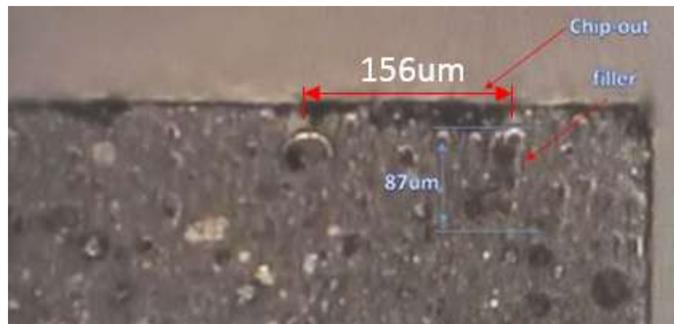

Fig. 1. Device A chip-out.

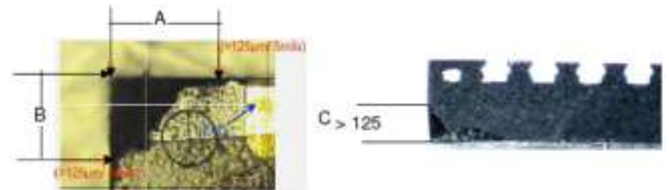

Fig. 2. Package chip-out specification.

- Parameter optimization, blade selection and evaluation, and ensuring planarity and calibration can help mitigate the package chip-out, still chip-out cannot be totally eliminated due to the degradation of the singulation blade

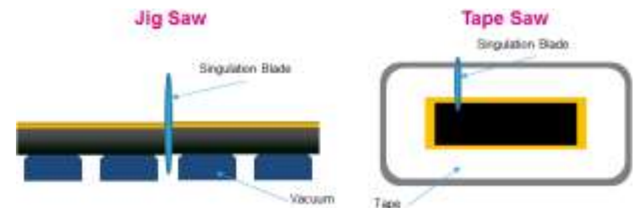

Fig. 3. Types of mechanical saw package singulation.

II. Design Solution

- The rejection caused by out-of-specs topside package chip-out could be eliminated through provision of indented design on the actual structure of the semiconductor integrated circuit (IC) package

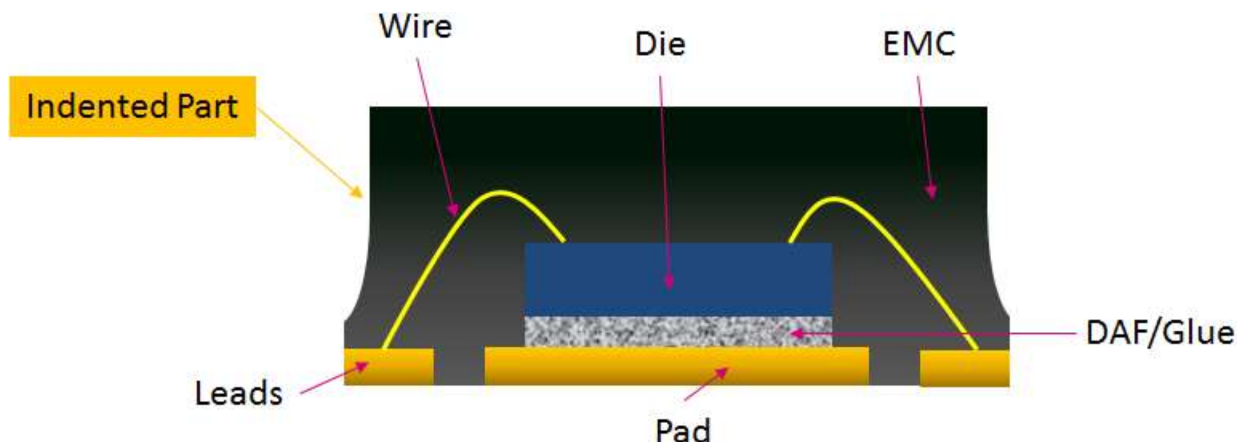

Fig. 4. Semiconductor IC package with indented sidewalls.

- The indented sidewalls are realized during mold encapsulation using modified and specialized design of the mold chase
- The lower part of the package without the indented design is the only part to be cut or sawn using mechanical blades during singulation process – prolonging the blade life