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Design and Simulation Study of Matching Networks of a Common-Source Amplifier

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Abstract— *This technical paper presents a design and study of impedance matching networks of a common-source amplifier, for Radio-Frequency (RF) applications. Input and output matching networks of the amplifier were designed and computed ensuring unconditional stability. Inductor parameters were computed and designed using Analysis and Simulation of Spiral Inductors and Transformers for ICs (ASITIC) and Integrated Spiral Inductor Calculator (SpiralCalc). Both software design tools are available for academic and research purposes. Impedance matching is necessary in RF circuit design to provide maximum possible power transfer between the input or source and the output or load. Design tradeoffs are inevitable and should be carefully handled when designing the impedance matching networks, to optimize the performance of the amplifier.*

Keywords—*Matching networks; impedance matching; RF; common-source amplifier; inductors.*

I. INTRODUCTION

Impedance matching offers a reliable solution in optimizing the performance of the Radio-Frequency Integrated Circuit (RFIC) design. Matching provides maximum power transfer between the input source and the output load. This allows the RF circuit to achieve the desired performance especially the gain requirements. Inductors and capacitors are key passive components that are crucial for impedance matching, and are specifically designed such that they would satisfy the gain requirements at a specific frequency or range of operation [1-4]. Design tradeoffs between matching network parameters are inevitable, so it is crucial that inductors and capacitors be designed carefully for the specific requirements of the intended application.

II. DESIGN METHODOLOGY

For this design and simulation study, actual S-parameters of a 300µm/0.25µm (Width/Length dimension) transistor (in *touchstone* format) were initially provided, for the common-source amplifier of RF application. Common-source amplifier is one of three basic topologies of single-stage transistor amplifier. This topology exhibits a relatively high input impedance white providing voltage gain and requiring a minimal voltage headroom [5-7]. Required values of S-parameters for a specific frequency of operation could then be determined using linear interpolation. Shown in Table I are the S-parameters of the transistor at frequency initially set to 2.6GHz.

TABLE I. S-Parameters of transistor at 2.6GHz (Polar).

S-Parameters	Magnitude	Angle
S_{11}	0.80705465	-41.9893745
S_{21}	1.16272657	100.8777943
S_{12}	0.07714536	28.9227451
S_{22}	0.41706929	-73.7682019

Stability conditions of the two-port network in terms of S-parameters play an essential role in amplifier designs. Although stability is frequency dependent, it is important that the amplifier design exhibits unconditional stability especially at higher frequencies.

There are several ways to check for the stability of the two-port network. The following stability constants given in Eq. (1) to Eq. (6) can be used to check for the stability of the design. These can also be used to compute for the source/generator and load reflection coefficients which will be discussed in succeeding section. Computed values are shown in Table II.

$$\Delta = det(S) = S_{11}S_{22} - S_{12}S_{21} \quad \text{Eq. (1)}$$

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\Delta|^2}{2|S_{12}S_{21}|} \quad \text{Eq. (2)}$$

$$B_1 = 1+|S_{11}|^2-|S_{22}|^2-|\Delta|^2 \quad \text{Eq. (3)}$$

$$B_2 = 1+|S_{22}|^2-|S_{11}|^2-|\Delta|^2 \quad \text{Eq. (4)}$$

$$C_1 = S_{11} - \Delta S_{22}^* \quad \text{Eq. (5)}$$

$$C_2 = S_{22} - \Delta S_{11}^* \quad \text{Eq. (6)}$$

B_1, B_2, C_1, C_2, and Δ are intermediate quantities, necessary for checking the stability of the transistor [6]. K is the Rollett stability factor, and must be greater than unity, that is $K > 1$, as well as one other condition to satisfy the unconditional stability of the transistor [6].

TABLE II. Stability constants.

Stability Constants	Values
Δ	$0.38253 \angle$-103.43156°
K	1.78957
B_1	1.33106
B_2	0.37628
C_1	$0.65208 \angle$-44.98328°
C_2	$0.13295 \angle$-103.48520°

Computed K is at 1.78957, which is greater than unity. Hence, any of the following criteria is sufficient and necessary for unconditional stability:

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$K > 1$ and $|\Delta| < 1$ Eq. (7)
$K > 1$ and $B_1 > 0$ Eq. (8)
$K > 1$ and $B_2 > 0$ Eq. (9)
$K > 1$ and $|S_{12}S_{21}| < 1 - |S_{11}|^2$ Eq. (10)
$K > 1$ and $|S_{12}S_{21}| < 1 - |S_{22}|^2$ Eq. (11)

Table III shows the condition values of all the unconditional stability criteria.

TABLE III. Unconditional stability criteria.

Criteria	Values	Condition
$K > 1$	1.78957 > 1	✓
$\|\Delta\| < 1$	0.38253 < 1	✓
$B_1 > 0$	1.33106 > 0	✓
$B_2 > 0$	0.37628 > 0	✓
$\|S_{12}S_{21}\| < 1 - \|S_{11}\|^2$	0.08970 < 0.34866	✓
$\|S_{12}S_{21}\| < 1 - \|S_{22}\|^2$	0.08970 < 0.82605	✓

It can be observed that all of the conditions are met. Therefore, the two-port network in terms of S-parameters is unconditionally stable. Shown in Fig. 1 is the circuit of a two-port network with input and output matching networks.

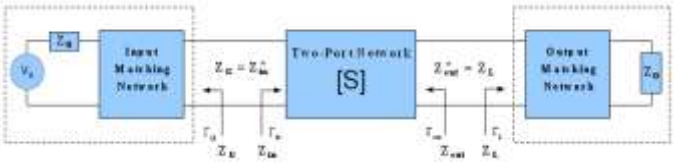

Fig. 1. L-network of the input matching network.

Maximum power transfer is achieved when both the generator and load are conjugately matched to the two-port network, that is,

$\Gamma_{in} = \Gamma_G^*$ and $\Gamma_{out} = \Gamma_L^*$ Eq. (12)

$Z_{in} = Z_G^*$ and $Z_{out} = Z_L^*$ Eq. (13)

Where

Γ_{in} = input reflection coefficient of the two-port network
Γ_{out} = output reflection coefficient of the two-port network
Γ_G = source or generator reflection coefficient
Γ_L = load reflection coefficient
Z_{in} = input impedance of the two-port network
Z_{out} = output impedance of the two-port network
Z_G = source or generator impedance
Z_L = load impedance

Through simultaneous conjugate matching, the following reflection coefficients can be obtained:

$$\Gamma_{in} = \Gamma_G^* = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = \frac{S_{11} - \Delta\Gamma_L}{1 - S_{22}\Gamma_L} \quad \text{Eq. (14)}$$

$$\Gamma_{out} = \Gamma_L^* = S_{22} + \frac{S_{12}S_{21}\Gamma_G}{1 - S_{11}\Gamma_G} = \frac{S_{22} - \Delta\Gamma_G}{1 - S_{11}\Gamma_G} \quad \text{Eq. (15)}$$

Source (or generator) and load reflection coefficients in Eq. (16) and (17) can also be derived using Eq. (3) to Eq. (6).

$$\Gamma_G = \frac{B_1 - \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad \text{Eq. (16)}$$

$$\Gamma_L = \frac{B_2 - \sqrt{B_2^2 - 4|C_2|^2}}{2C_2} \quad \text{Eq. (17)}$$

Using the expressions in Eq. (16) and (17), source/generator and load impedances can now be obtained.

$$Z_G = \left(\frac{1+\Gamma_G}{1-\Gamma_G}\right) Z_0 \quad \text{Eq. (18)}$$

$$Z_L = \left(\frac{1+\Gamma_L}{1-\Gamma_L}\right) Z_0 \quad \text{Eq. (19)}$$

Table IV shows the values of all the reflection coefficients as well as the impedances, assuming normalization impedance of $Z_0 = 50\ \Omega$.

TABLE IV. Reflection coefficients and impedances.

Γ and Z	Values
Γ_{in}	0.57750 - j0.57717
Γ_{out}	-0.09650 - j0.40242
Γ_G	0.57750 + j0.57717
Γ_L	-0.09650 + j0.40242
Z_{in}	32.57934 - j112.81061 Ω
Z_{out}	30.37350 - j29.497274 Ω
Z_G	32.57934 - j112.81061 Ω
Z_L	0.57750 - j0.57717

Now, for the input and output matching networks, L-network is used because it is the simplest and most widely used matching network for lumped elements [6] [8]. Circuit diagram is shown in Fig. 2 and 3.

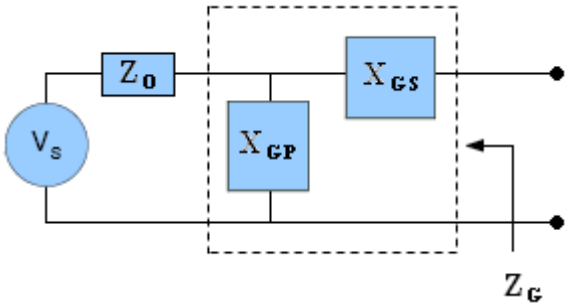

Fig. 2. L-network of the input matching network.

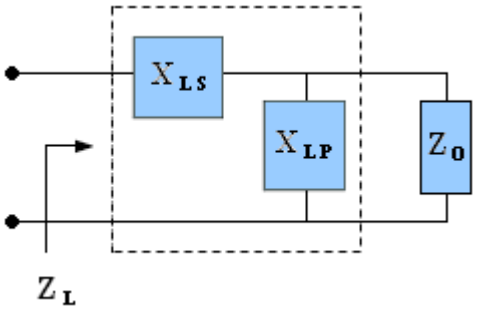

Fig. 3. L-network of the output matching network.

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Where

X_{GS} = series reactance of the L-network of the input matching network

X_{GP} = parallel reactance of the L-network of the input matching network

X_{LS} = series reactance of the L-network of the output matching network

X_{LP} = parallel reactance of the L-network of the output matching network

The elements of the L-network for both the input and output matching network as shown in Fig. 2-3 are arranged in such orientation given that the real components of Z_G and Z_L (or R_G and R_L) are smaller than the real component of the normalization impedance which is Z_0 = 50 Ω (or R_0 = 50 Ω) [6]. To verify,

$R_G = 32.57934\,\Omega < R_0 = 50\,\Omega$ Eq. (20)

$R_L = 30.37350\,\Omega < R_0 = 50\,\Omega$ Eq. (21)

For the L-network of the input matching network, the elements can be solved using the following equations given that Z_0 = 50 Ω (R_0 = 50 Ω, X_0 = 0):

$$Q_G = \sqrt{\frac{R_0}{R_G} - 1} \quad \text{Eq. (22)}$$

$$X_{GP} = \pm\frac{R_0}{Q_G} \quad \text{Eq. (23)}$$

or $$X_{GP1} = +\frac{R_0}{Q_G} \quad \text{Eq. (24)}$$

$$X_{GP2} = -\frac{R_0}{Q_G} \quad \text{Eq. (25)}$$

$$X_{GS} = -\left(-X_G \pm R_G Q_G\right) \quad \text{Eq. (26)}$$

or $$X_{GS1} = -\left(-X_G + R_G Q_G\right) \quad \text{Eq. (27)}$$

$$X_{GS2} = -\left(-X_G - R_G Q_G\right) \quad \text{Eq. (28)}$$

Also, for the L-network of the output matching network, the elements can be solved using the following equations given that Z_0 = 50 Ω (R_0 = 50 Ω, X_0 = 0):

$$Q_L = \sqrt{\frac{R_0}{R_L} - 1} \quad \text{Eq. (29)}$$

$$X_{LP} = \pm\frac{R_0}{Q_L} \quad \text{Eq. (30)}$$

or $$X_{LP1} = +\frac{R_0}{Q_L} \quad \text{Eq. (31)}$$

$$X_{LP2} = -\frac{R_0}{Q_L} \quad \text{Eq. (32)}$$

$$X_{LS} = -\left(-X_L \pm R_L Q_L\right) \quad \text{Eq. (33)}$$

or $$X_{LS1} = -\left(-X_L + R_L Q_L\right) \quad \text{Eq. (34)}$$

$$X_{GS2} = -\left(-X_L - R_L Q_L\right) \quad \text{Eq. (35)}$$

Table V tabulates computed values obtained Eq. (22) to Eq. (35).

TABLE V. L-Network elements.

Q and X	Values
Q_G	0.73124
X_{GP1}	68.37681 Ω
X_{GP2}	-68.37681 Ω
X_{GS1}	88.98723 Ω
X_{GS2}	136.63400 Ω
Q_L	0.80385
X_{LP1}	62.20081 Ω
X_{LP2}	-62.20081 Ω
X_{LS1}	5.08159 Ω
X_{LS2}	53.9129 Ω

Actual inductor and capacitor values at f = 2.6GHz can be computed from the L-network reactances. Positive reactance denotes an inductive component while a negative reactance implies a capacitive component. The values of the actual passive components are summarized in Table VI.

TABLE VI. Actual L-Network Elements.

L and C	Values
L_{GP1}	4.1856 nH
C_{GP2}	0.8952 pF
L_{GS1}	5.4472 nH
L_{GS2}	8.3638 nH
L_{LP1}	3.8075 nH
C_{LP2}	0.9841 pF
L_{LS1}	0.3111 nH
L_{LS2}	3.3002 nH

Two sets of values will be used in the simulation to check if the whole circuit is really matched at the frequency of operation which is 2.6GHz. Design1 is comprised of L_{GS1} and L_{GP1} for the input matching network and L_{LS1} and L_{LP1} for the output matching network. On the other hand, Design2 is composed of L_{GS2} and C_{GP2} for the input matching network and L_{LS2} and C_{LP2} for the output matching network.

III. Simulation Results and Analysis

Total of four designs (Design1a, Design1b, Design2a, and Design2b) were studied, designed, and simulated using the two sets of values of the input and output matching networks.

Design1a and Design2a uses ideal inductors with the two sets of values, respectively, while Design1b and Design2b uses S-parameters and *n2port* model for inductors. Fig. 4 and Fig. 5 shows the schematic circuit designs of Design1a and Design2a using ideal inductors, with n2port model for the transistor.

Software design tools namely Analysis and Simulation of Spiral Inductors and Transformers for ICs (ASITIC) [9], [10] and Integrated Spiral Inductor Calculator (SpiralCalc) [11], [12] were used for the design of inductors for Design1b and

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Design2b. These tools are available for academic and research purposes. SpiralCalc models are based on computations and studies conducted in [12-14]. Table VII and VIII shows the design parameters obtained for the design of the inductors using the two tools. Fig. 6 shows the schematic circuit design for both Design1b and Design2b. The *n2port* from the *analogLib* library is used for the two-port network model of the inductors and also for the transistor.

In ASITIC, the inductors were designed such that desired inductances are achieved and the Q-factors optimized. All of the inductors have Q-factor of at least 5 except for L_{LS1} because of its low inductance value. For the inductor design using SpiralCalc, same parameter values from the ASITIC parameters were used except for the length or diameter of the inductor inductor. The lengths are tweaked such that the desired inductances are achieved for the inductors.

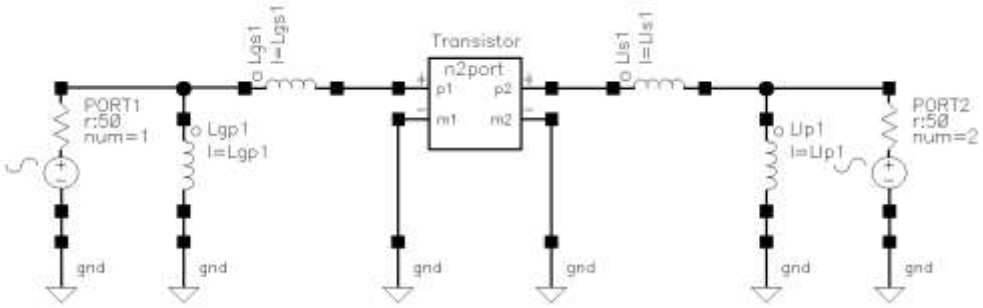

Fig. 4. Design1a schematic.

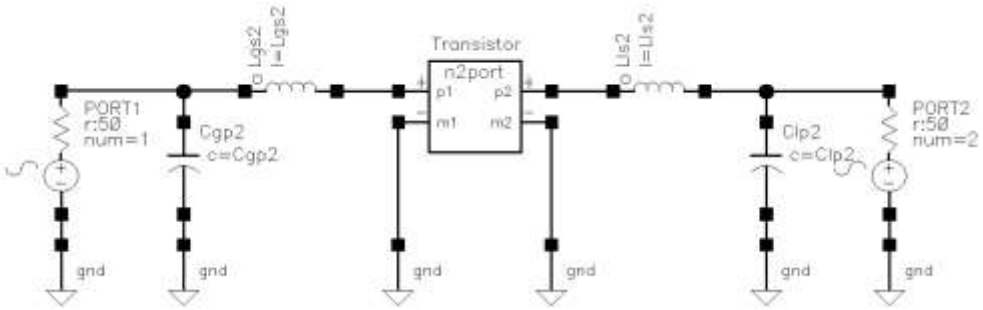

Fig. 5. Design2a schematic.

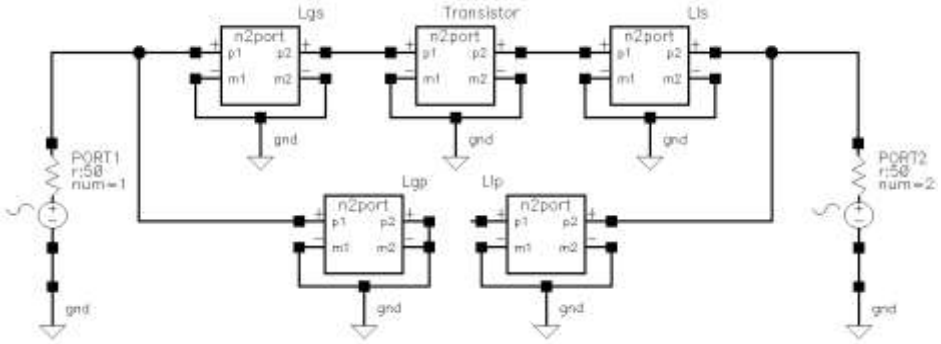

Fig. 6. Design1b/2b using *n2port* model for the inductors.

TABLE VII. Inductor Design Using ASITIC.

Parameters	Inductors					
	L_{GP1}	L_{GS1}	L_{LP1}	L_{LS1}	L_{GS2}	L_{LS2}
Desired inductance	4.1856 nH	5.4472 nH	3.8075 nH	0.3111 nH	8.3638 nH	3.3002 nH
No. of sides	8	8	8	8	8	8
Length/diameter, D	250 µm	250 µm	250 µm	180 µm	250 µm	250 µm
Metal width, W	10.7594 µm	10.8155 µm	11.8642 µm	11.0343 µm	10.4277µm	11.7276 µm
Spacing, S	1 µm	1 µm	1 µm	1 µm	1 µm	1 µm
No. of turns, N	4	5	4	1	8	3.5
Metal layer	5	5	5	5	5	5
Inductance, L	4.1856 nH	5.4472 nH	3.8075 nH	0.3111 nH	8.3638 nH	3.3002 nH
Q-factor	5.9517	6.0689	6.0507	2.8124	5.4851	5.9519

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TABLE VIII. Inductor Design Using SpiralCalc.

Parameters	Inductors					
	L_{GP1}	L_{GS1}	L_{LP1}	L_{LS1}	L_{GS2}	L_{LS2}
Desired inductance	4.1856 nH	5.4472 nH	3.8075 nH	0.3111 nH	8.3638 nH	3.3002 nH
No. of sides	8	8	8	8	8	8
Length/diameter, D	223.679 µm	228.409 µm	222.333 µm	151.5 µm	237.511 µm	221.56 µm
Metal width, W	10.7594 µm	10.8155 µm	11.8642 µm	11.0343 µm	10.4277µm	11.7276 µm
Spacing, S	1 µm	1 µm	1 µm	1 µm	1 µm	1 µm
No. of turns, N	4	5	4	1	8	3.5
Inductance, L:						
Modified Wheeler	4.186 nH	5.447 nH	3.808 nH	0.311 nH	8.364 nH	3.300 nH
Current Sheet	4.188 nH	5.516 nH	3.828 nH	0.319 nH	8.777 nH	3.296 nH
Monomial Fit	4.292 nH	5.578 nH	3.927 nH	0.342 nH	8.530 nH	3.406 nH

The *n2port* from the *analogLib* library is used for the two-port network. Although *spectre*-format file is preferred for the S-parameter file input of the *n2port* component, *touchstone*-format can still be used. In this paper, the *touchstone*-format S-parameter file is used since the actual S-parameters are given in *touchstone* format. Still, *touchstone*-formatted file can be converted to *spectre*-format using the command *sptr*.

Fig. 7-14 shows the comparison of the results of the S-parameter plots of all four designs, which are summarized in Table IX and X.

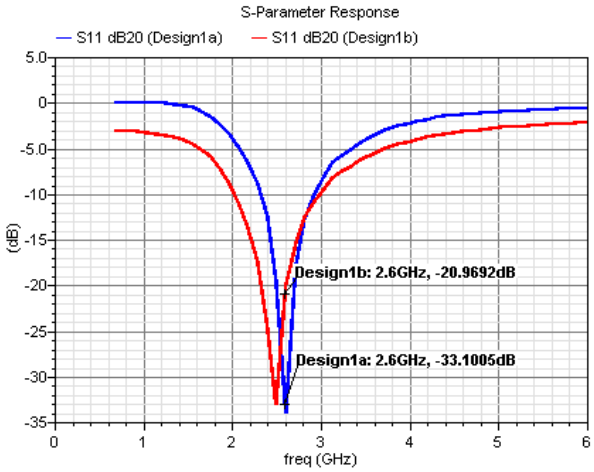

Fig. 7. S_{11} plot of Design1a and Design1b.

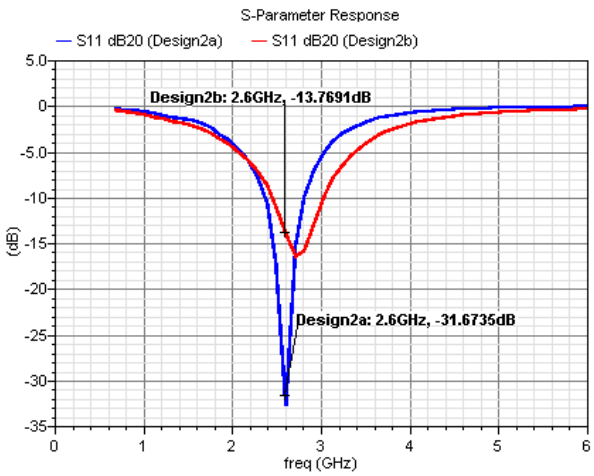

Fig. 8. S_{11} plot of Design2a and Design2b.

S-parameter plots were obtained using the *sp* analysis. It can be shown in Fig. 7, 8, 13 and 14 that the designs are somehow matched at frequency 2.6GHz The values obtained from the simulations using *n2port* for the inductors (Design1b and Design2b) are worse than the results achieved using ideal passive components (Design1a and Design2a). The reason for this is simply because of ideality – ideal designs produce ideally better results.

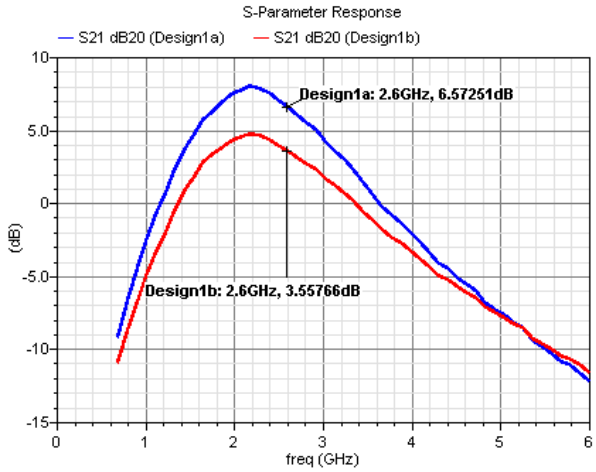

Fig. 9. S_{21} plot of Design1a and Design1b.

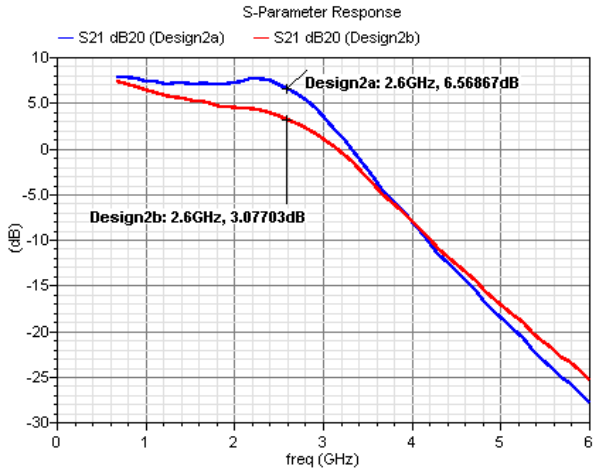

Fig. 10. S_{21} plot of Design2a and Design2b.

It can be observed that the S-parameter plots of Design2 (a and b) are smoother than the plots of Design1 (a and b) at frequencies greater than 2.6GHz. The difference is evident

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especially in the S_{22} plots. This signifies that Design2, which is comprised of inductor-capacitor combination in the L-matching networks, exhibits a more stable behavior for higher frequencies than the Design1 which is an all-inductor design. Moreover, the S_{11} and S_{22} plots of Design2 are more symmetric in reference to the frequency of operation which is at 2.6GHz compared to Design1.

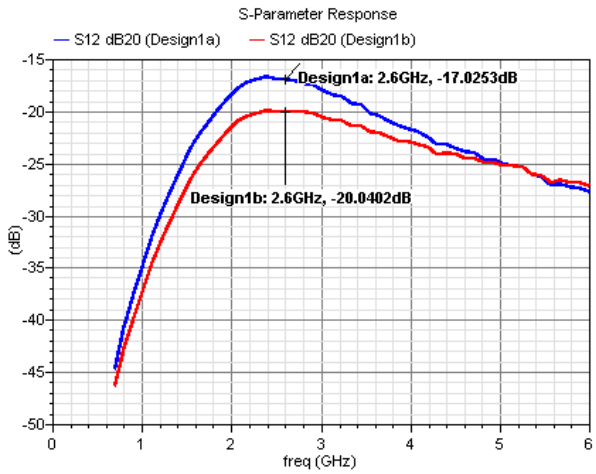

Fig. 11. S_{12} plot of Design1a and Design1b.

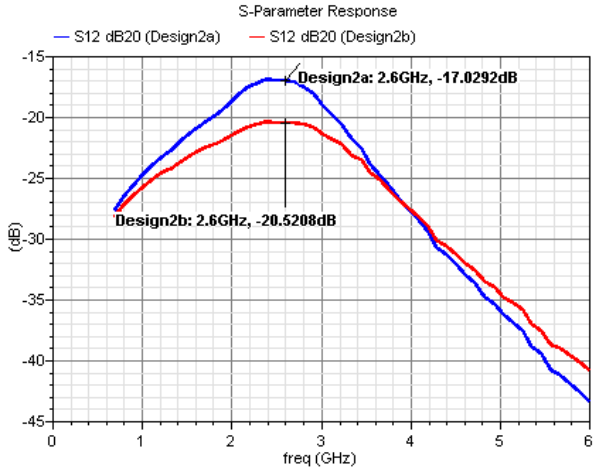

Fig. 12. S_{12} plot of Design2a and Design2b.

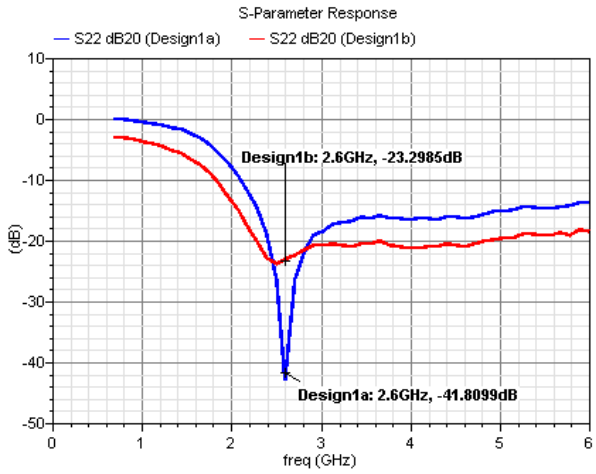

Fig. 13. S_{22} plot of Design1a and Design1b.

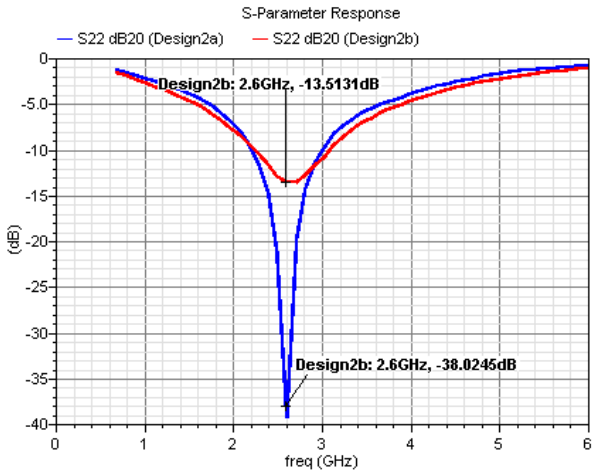

Fig. 14. S_{22} plot of Design2a and Design2b.

The gain of the amplifier is shown in the S_{21} plots in Fig. 7-8. At frequency 2.6GHz, the gain is at 6.5725dB for the Design1a and 6.5687dB for the Design2a. If the gain-bandwidth product is to be remained constant, then as the bandwidth or the frequency increases, the gain should compensate, thus decreasing the gain at higher frequencies. In addition, the gain of the amplifier degrades more in Design1b and Design2b because of the use of a non-ideal component which is the *n2port* instead of an ideal inductor.

TABLE IX. S-Parameters response of Design1 at 2.6GHz.

S-Parameters	Design1a	Design1b
S_{11}	-33.1005 dB	-20.9692 dB
S_{21}	6.57251 dB	3.55766 dB
S_{12}	-17.0253 dB	-20.0402 dB
S_{22}	-41.8099 dB	-23.2985 dB

TABLE X. S-Parameter Response of Design2 at 2.6GHz.

S-Parameters	Design2a	Design2b
S_{11}	-31.6735 dB	-31.6735 dB
S_{21}	6.56867 dB	3.07703 dB
S_{12}	-17.0292 dB	-20.5208 dB
S_{22}	-38.0245 dB	-13.5131 dB

Noise figure analysis was also simulated for all designs, with results summarized in Table XI. Based on the results, Design1b and Design2b have poorer noise performance than that of Design1a and Design2a. This is because *n2port* adds to the total noise of the circuit.

TABLE XI. Noise figure at 2.6GHz.

Design	Noise Figure
Design1a	3.04176 dB
Design1b	4.05858 dB
Design2a	3.04199 dB
Design2b	3.56663 dB

Fig. 15-26 shows the S-parameter plots in Smith charts.

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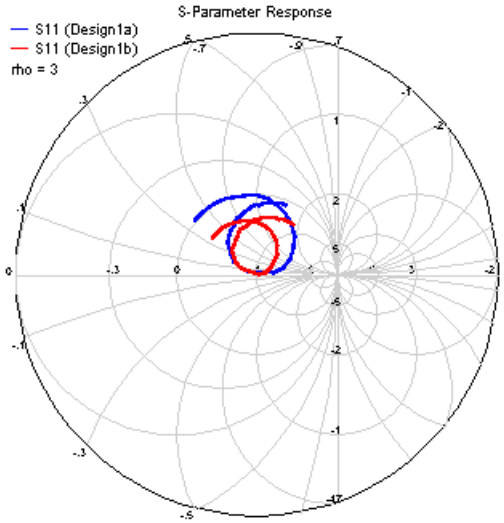

Fig. 15. S_{11} impedance Smith chart plots of Design1.

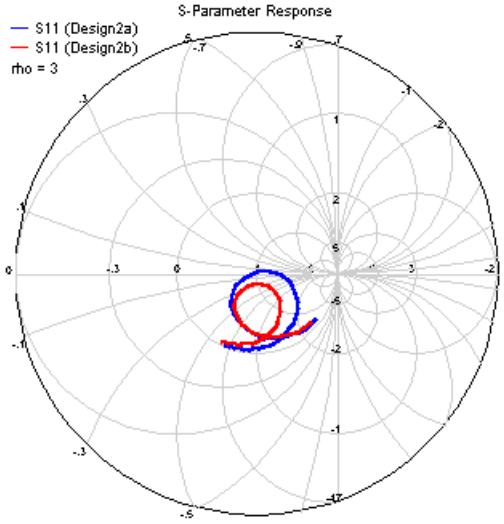

Fig. 16. S_{11} impedance Smith chart plots of Design2.

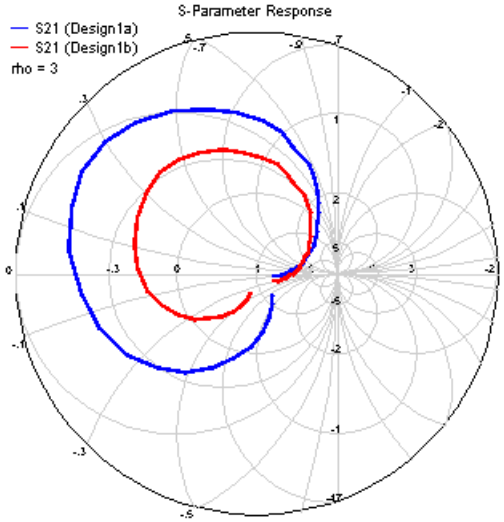

Fig. 17. S_{21} impedance Smith chart plots of Design1.

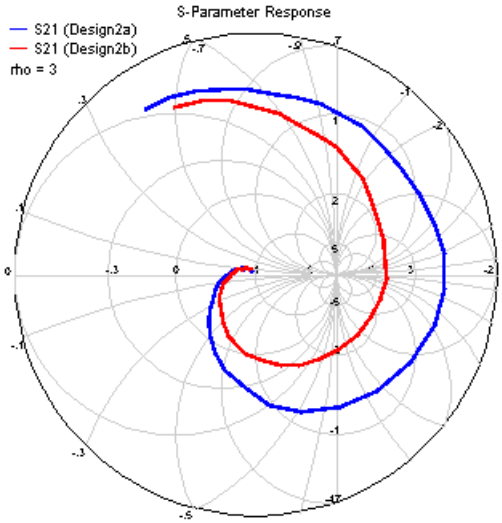

Fig. 18. S_{21} impedance Smith chart plots of Design2.

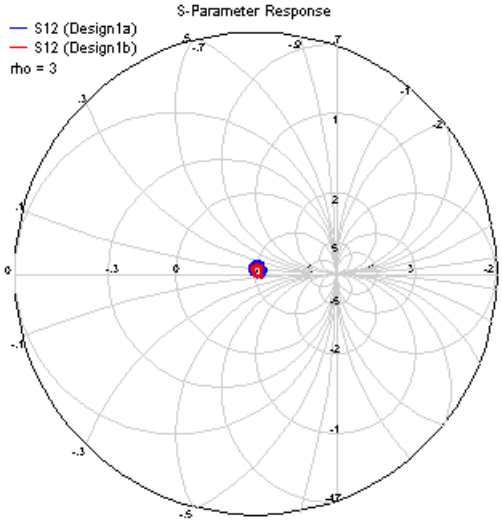

Fig. 19. S_{12} impedance Smith chart plots of Design1.

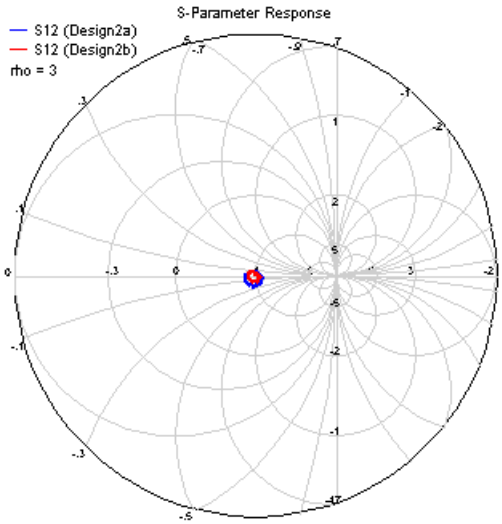

Fig. 20. S_{12} impedance Smith chart plots of Design2.

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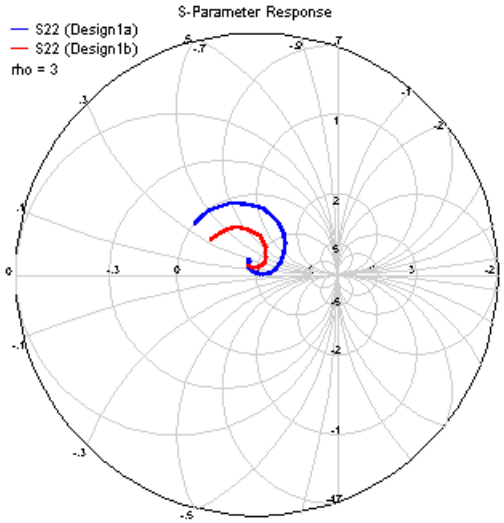

Fig. 21. S_{22} impedance Smith chart plots of Design1.

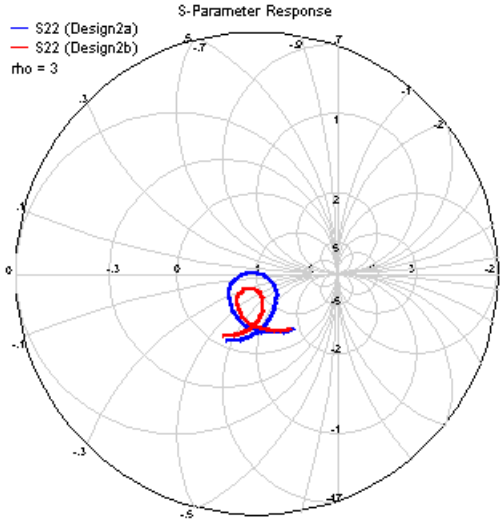

Fig. 22. S_{22} impedance Smith chart plots of Design2.

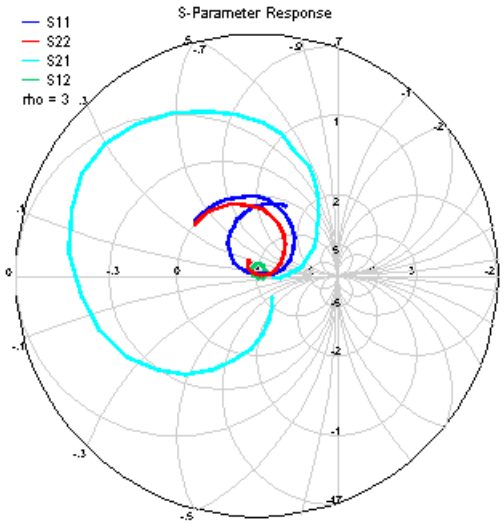

Fig. 23. Impedance Smith chart plots of Design1a.

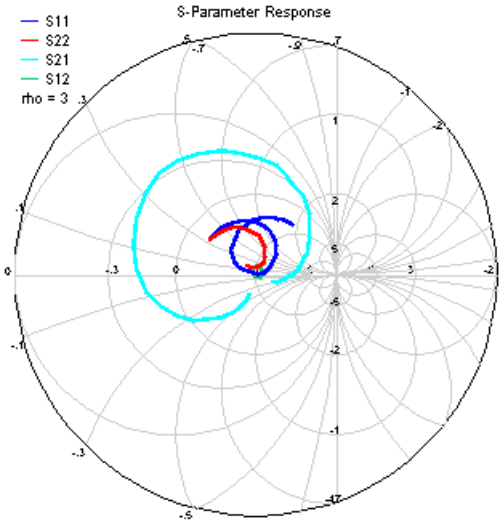

Fig. 24. Impedance Smith chart plots of Design1b.

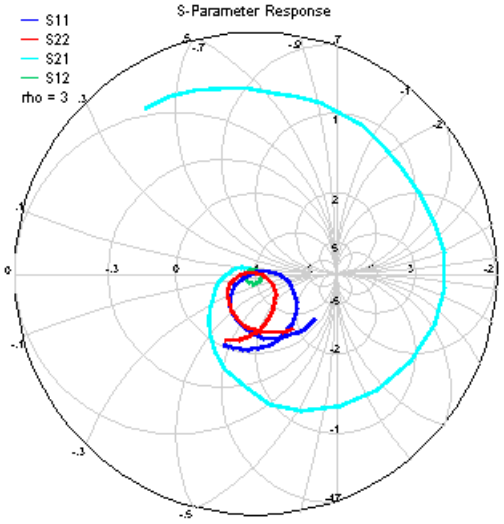

Fig. 25. Impedance Smith chart plots Design2a.

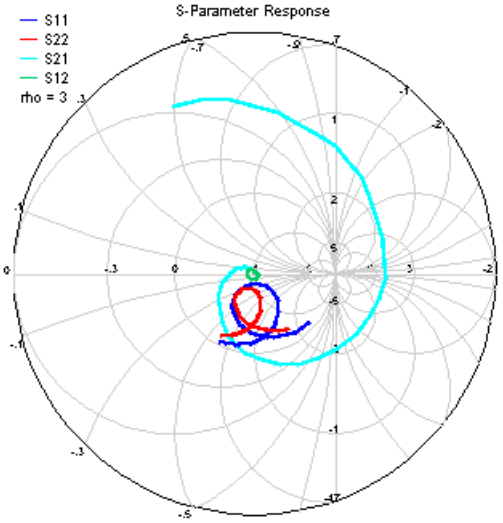

Fig. 26. Impedance Smith chart plots of Design2b.

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Since both Design1a and Design1b are an all-inductor designs, the responses of S-parameters in the impedance Smith chart are more on the inductive half the Smith chart as shown in Fig. 15, 17, 19, 21, 23 and 24. On the other hand, Design2a and Design2b have capacitors in their matching networks, thus the impedance Smith chart responses of the S-parameters are more on the capacitive half of the Smith chart as shown in Fig. 16, 18, 20, 22, 25 and 26.

IV. Conclusions and Recommendations

Matching is necessary in RF circuit design to provide maximum power transfer between the source or generator and the output or load. In this design and study, two designs with two implementations for each design were modeled and investigated. The design (Design1b and Design2b) which comprised of an inductor-capacitor combination in the input and output matching networks resulted to a smoother response or a more stable behavior for higher frequencies than the design (Design1a and Design2a) with all inductors in the matching networks. Moreover, the values achieved from the simulations using ideal inductors (Design1a and Design2b) are better than the results obtained from using *n2port* (Design1b and Design2b) which is a non-ideal component. Furthermore, *n2port* introduces noise to the system, thus, adding to the total noise figure of the circuit. The designs that use ideal components tend to produce better results than using non-ideal components.

Complex tradeoffs among technology specifications and design parameters exist and should be carefully handled when designing the impedance matching networks, to optimize the performance of the RF circuit. Design and study of particular passive components could be helpful in understanding and finally designing the matching networks.

For future research, physical implementations of the impedance matching networks could be studied in order to improve and optimize the simulated models.

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