International Research Journal of Advanced Engineering and Science
ISSN: 2455-9024

Modified SEPIC PFC Converter for Improved Power Factor and Low Harmonic Distortion

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***Abstract*—** *The theoretical and experimental analysis of the modified SEPIC converter is presented in this paper. The proposed converter operates in DCM. As the converter operates in DCM it acts as a voltage follower ie the input current follows the input current. The voltage across the switch is reduced. Moreover a digital control technique is used to reduce the third harmonic input current distortion. Finally, 100W power factor correction circuit was developed with an operational efficiency of 95%.*

I. INTRODUCTION

Power factor is the ratio of true power to apparent power or power factor is the cosine of angle between voltage and current in a circuit. When the current and voltage are in phase, then the power factor is unity. Most of the loads in a domestic household circuit are inductive in nature and hence have low lagging power factor. With low power factor loads, the current flowing through electrical system components is higher. The excessive currents results in heating, which can damage or shorten the life of equipment. The low power factor is highly undesirable as it causes an increase in current, resulting in additional losses due to I^2R power loss in all the elements of power system from power station generator down to the utilization devices. Power factor is a measure of how effectively the current is being converted into useful work output and more particularly is a good indicator of the effect of the load current on the efficiency of the supply system. A distorted current waveform can be the result of a rectifier, variable speed drive, switched mode power supply, discharge lighting or other electronic load. Power factor correction attempts to adjust the power factor of an AC load or an AC power transmission system to unity (1.00) through various methods. Both active and passive power factor correction circuits can be used to improve the power factor. In this paper an active power factor correction circuit is used. Using active power factor correction reduces the cost and bulkiness of the circuit.

The usual solution is a boost converter pre-regulator operating in DCM. It is a simple and cost effective method because in DCM it works as a voltage follower. The operation in DCM reduces the commutation losses. This solution is limited for low-power applications due to an increased converter conduction losses operating in DCM. Since the input inductor of the boost converter operates in DCM, a high-frequency filter composed by an inductor and capacitor must be used in the preregulator input in order to reduce the current ripple at the input and the problem presented by the boost preregulator operating in DCM is the input current distortion.

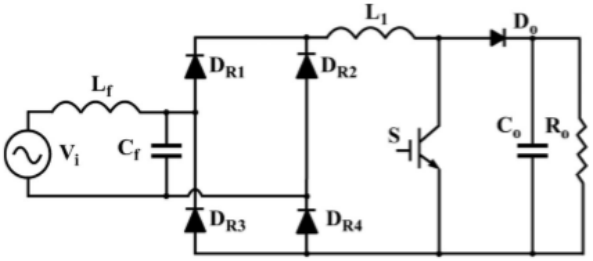

Fig. 1. Boost converter.

The voltage applied across the input inductor during its demagnetization is equal to the difference of the output voltage and the input voltage; hence, the current distortion increases when the difference between the output voltage and the peak input voltage is reduced. Therefore, the output voltage must be increased for reducing the third-harmonic input current distortion and improving the power factor. The boost converter can operate with power factor as unity independently of the difference between the output and input voltage operating at the boundary of the DCM and continuous conduction mode (CCM) with a variable switching frequency modulation. The classical SEPIC converter, shown in figure 2, presents a step-up/step-down static gain and usually isused as a high power factor preregulator in applications where the output voltage is lower than the peak of the ac input voltage.

The preregulator using the classical SEPIC converter in DCM presents two additional operation characteristics. Firstly, the converter operates as a voltage follower (DCM) with a low value for the inductor L_2 and using a high value for the inductor L_1, but the input current presents a low current ripple just as a boost power factor rectifier operating in CCM with current-control loop.

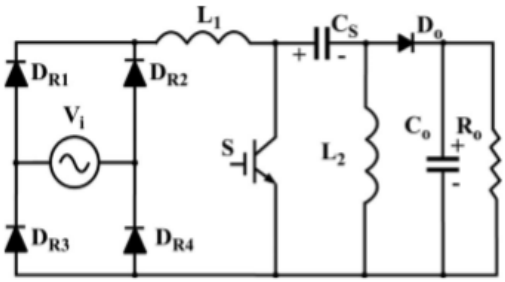

Fig. 2. Classical SEPIC Converter.

Consequently, the L_f–C_f filter used in the boost converter in DCM is not required in the SEPIC converter operating in DCM. Therefore, the number of components for both

Amrutha M P and Priya G Das, "Modified SEPIC converter for improved power factor and low harmonic distortion," *International Research Journal of Advanced Engineering and Science*, Volume 1, Issue 4, pp. 223-227, 2016.

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converters operating in DCM is equal. But, in a practical application, an electromagnetic interference (EMI) filter is necessary as in any rectifier circuits. The second important characteristic using the SEPIC converter in DCM is that it acts as a voltage follower. The third-harmonic distortion is not presented because the inductor L_2 is demagnetized with the output voltage.

The modified SEPIC dc–dc has an additional diode DM and capacitor (CM) at the classical SEPIC converter, the inclusion of the diode and the capacitor reduces the switch voltage and provides additional advantages. The modified SEPIC converter operates as a voltage follower and the input current presents low current ripple such as a classical SEPIC converter, designing the converter in DCM and using a low value for the inductor L_2 and a high value for the inductor L_1.

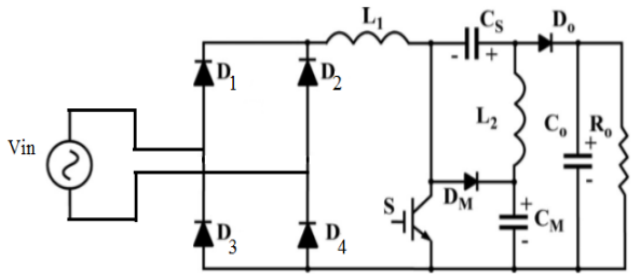

Fig. 3. Modified SEPIC Converter.

The modified SEPIC converter operating in Discontinuous Conduction Mode (DCM) presents three operational stages. For analysis the steady state operation is considered and all the components are assumed to be ideal. The voltages across all the capacitors are considered constant during a switching period. In DCM operation when the power switch is turned off the currents in all diodes of the circuit are equal to zero. Therefore, the DCM operation occurs when D_O and D_M diodes are not conducting before the switch is turn-on. It has a diode bridge and an ac source at the input side. High value of the input inductor L_1 is chosen to reduce the input current ripple. Inductor L_2 is kept low so as to operate it as a voltage follower. At steady state the voltage across both the inductors are zero and the sum of the input voltage V_{in} and capacitor C_S voltage is equal to the capacitor C_M voltage.

II. THEORITICAL ANALYSIS

The three operation stages of Modified SEPIC in DCM are presented as follows:

$$V_{C_M} = V_{in} + V_{C_S} \tag{1}$$

1) First Stage [$t_0 - t_1$]:

When the power switch S is turned ON, the input inductor L_1 stores energy and full voltage comes across the inductor (V_{L1}). The voltage across the inductor L_2 (V_{L2}) is equal to the voltage across the capacitor C_M minus the voltage across the capacitor C_S. This difference in voltage is equal to the input voltage as presented in equation (1). The currents through inductors L_1 and L_2 are increasing, but since L_2 is lower than L_1, the current variation in L_2 is higher than in L_1. The diodes D_M and D_O does not conducts during this period.

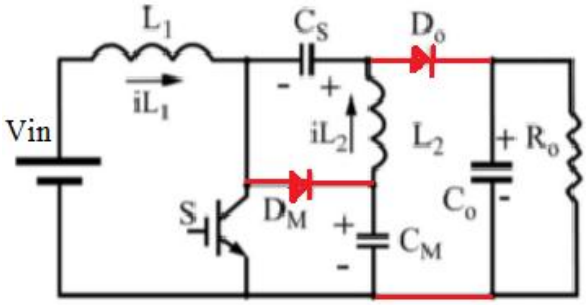

Fig. 4. First operating stage.

$$V_{L_1} = V_{L_2} = V_{in} \tag{2}$$

$$\Delta i_{L_1} = \frac{V_{in} \times D}{L_1 \times f} \tag{3}$$

$$\Delta i_{L_2} = \frac{V_{in} \times D}{L_2 \times f} \tag{4}$$

2) Second operating Stage [$t_1 - t_2$]:

At t_1, the power switch S is turned OFF and the stored energy in the input inductor L_1 is transferred to the output through the C_S capacitor and output diode Do. The energy is also transferred to the C_M capacitor through diode D_M and the maximum switch voltage is equal to the C_M capacitor voltage. The energy stored in inductor L_2 is also transferred to the output and the capacitor C_S through the diodes D_O and D_M. The voltage across L_1 is equal to C_M capacitor voltage minus the input voltage and this difference is equal to the C_S capacitor voltage as calculated by (1). As the inductor dissipates energy the voltage across the inductor L_2 is equal to the negative of the capacitor voltage C_S. Thus, the voltage across the inductor L_1 and L_2 are equal to the negative capacitor C_S voltage during this stage. The time interval (t_2–t_1) is defined as t_d and is equal to the transference period of the energy stored in inductors L_1 and L_2 through diodes D_o and D_M . When current through L_1 and L_2 are equal with the same direction, the currents through the diodes D_o and D_M becomes zero, thus finishing this operation stage. Therefore, t_d is the conduction time of diodes D_M and D_o, where the energy stored in the inductors L_1 and L_2 is transferred.

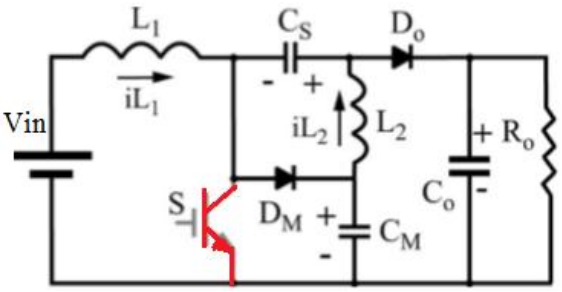

Fig. 5. Second operating stage.

$$V_{L_1} = V_{L2} = -V_{C_S} \tag{5}$$

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3) Third Stage [$t_3 - t_4$]:

The diodes D_o and D_M are blocked during the instant t_3 and the voltage across the inductors L_1 and L_2 are zero, maintaining the current through them as constant. The currents through the inductors L_1 and L_2 are same. The third stage is finished when the power switch S is turned ON at the instant where $t = t_4$, thus returning to the first operating stage.

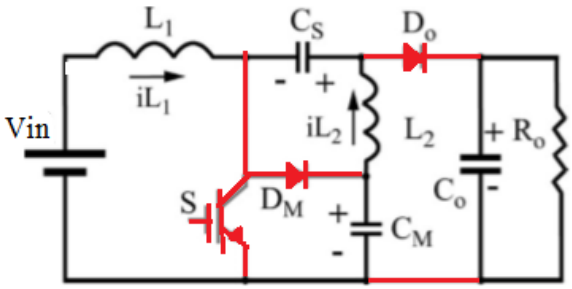

Fig. 6. Third operating stage.

The maximum switch voltage is equal to the capacitor C_M voltage, and this voltage is very much lower than the output voltage. The average current through the L_1 inductor is equal to the input current and the average current through the L_2 inductor is equal to the output current. The average current in the capacitors C_S and C_M are zero under steady state; thus, the average current of diodes D_M and D_o are equal to the output current.

III. THIRD-HARMONIC REDUCTION TECHNIQUE

The classical boost rectifier operating in DCM and the modified SEPIC rectifier contains a third-harmonic distortion at the input current. This current distortion is a function of the voltage difference between the input and output voltage. Normally, the output voltage is increased in order to reduce the third-harmonic distortions at the input curent and to maintain high power factor, but the semiconductors losses are increased. For a relatively low output voltage, only the information of the input and output voltage are necessary to define a duty-cycle variation in a line voltage half period, reducing the third-harmonic distortion. The same open-loop technique is utilized in this paper for the modified SEPIC converter by using a digital implementation for obtaining a High Power Factor.

The block diagram of the digital control implementation is shown in figure 7, including the third-harmonic reduction technique. Only the output and input voltages are necessary to control the pre-regulator to define a duty cycle variation. The output voltage is sampled and it is compared to an output voltage reference and the error signal obtained is applied to a PI voltage controller. Simultaneously, the sampled rectified input voltage and the output voltage reference are applied to a third harmonic reduction block in order to calculate the duty-cycle variation for the third-harmonic reduction. The result of the PI output voltage controller and the result of the third-harmonic reduction are multiplied obtaining the pre-regulator duty cycle and it is given to the PWM modulator thus generating the PWM signal that controls the Power switch S.

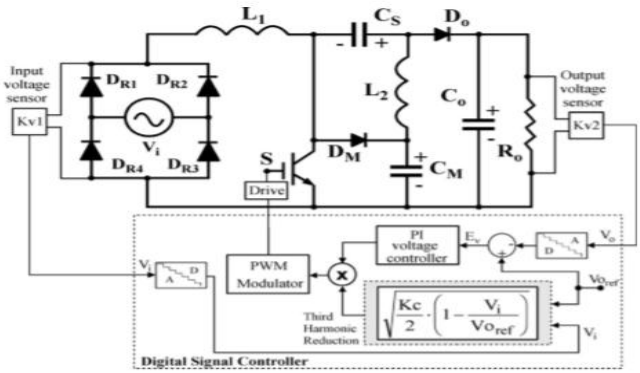

Fig. 7. Block Diagram of preregulator.

Design Parameters

Nominal input voltage *(Virms)*	127V
Output voltage Vo	400V
Output power Po	100W
Switching frequency(fs)	30KHz
Line frequency	50Hz
Maximum input currentt ripple	25%of the peak current
Inductor L1	6.8mH
Inductor L2	540µH
Capacitor Cs	220nF
Capacitor CM	220nF
Capacitor Co	120µF
Diodes DM-Do	UF5408
Duty ratio	0.38

IV. MATLAB SIMULATION

The Power factor correction converter known as the Modified SEPIC converter were simulated using Matlab softaware and the following results were obtained. The converter performance with (third harmonic distortion technique) and without were compared and the following conclusion were obtained. The FFT analysis was done to calculate the harmonic distortions. In the Modified SEPIC converter the harmonic distortion was about 9% and by the inclusion of a third harmonic reduction block the harmonic distortion in the input current was reduced to a value less than 5%, which is in the acceptable range.

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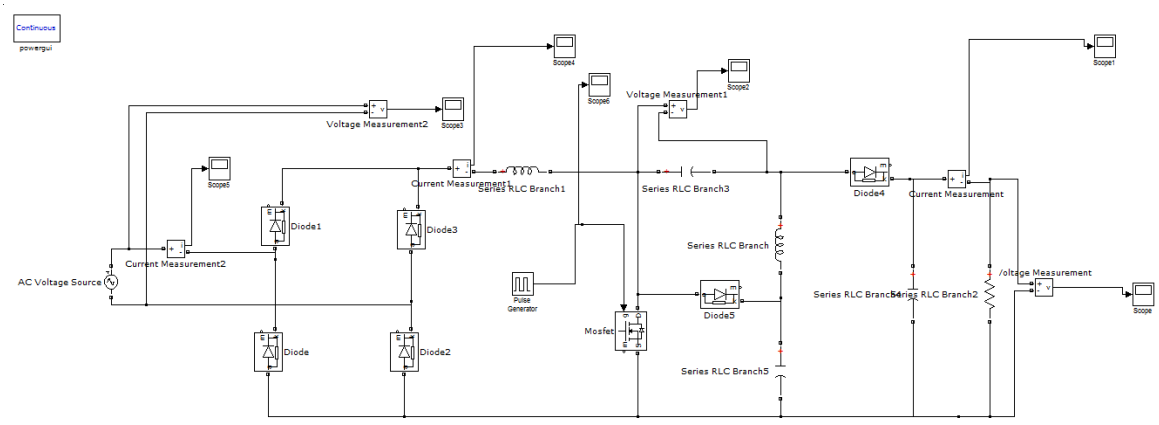

Fig. 8. Matlab simulation of modified SEPIC converter.

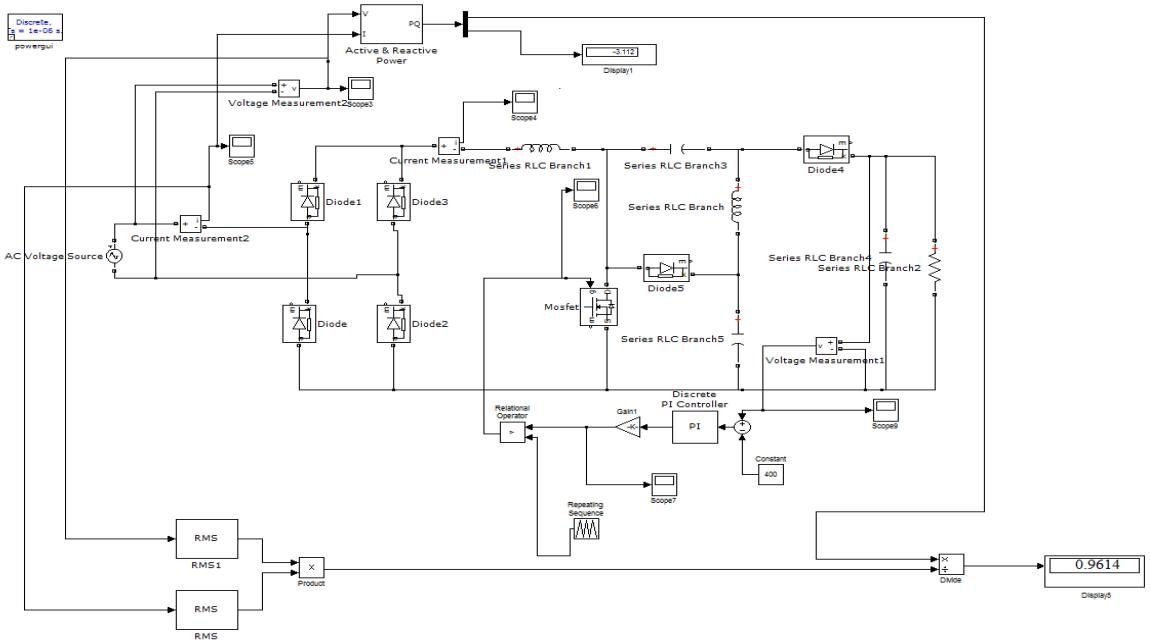

Fig. 9. Matlab simulation of the modified SEPIC converter wth third harmonic reduction technique.

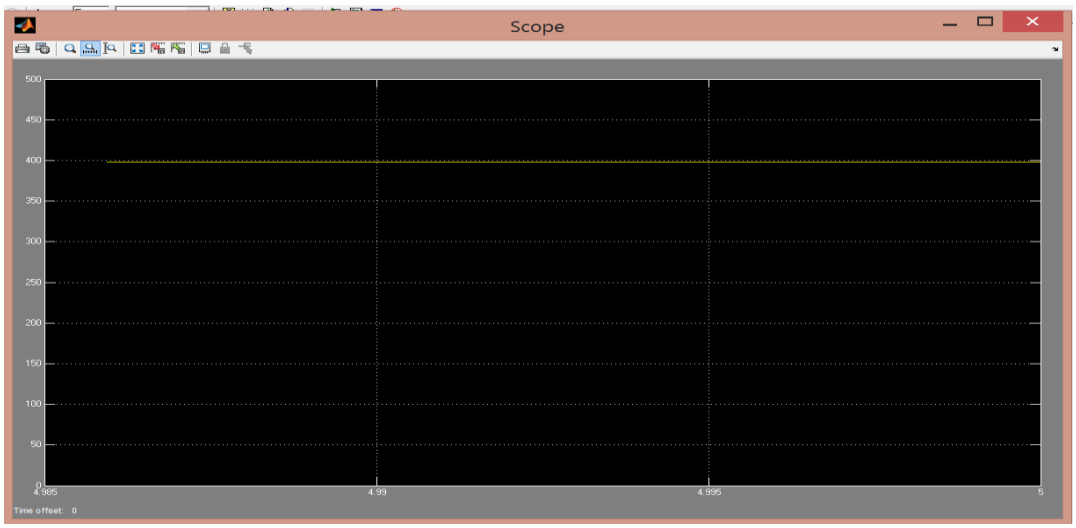

Fig. 10. Output voltage of the modified SEPIC converter.

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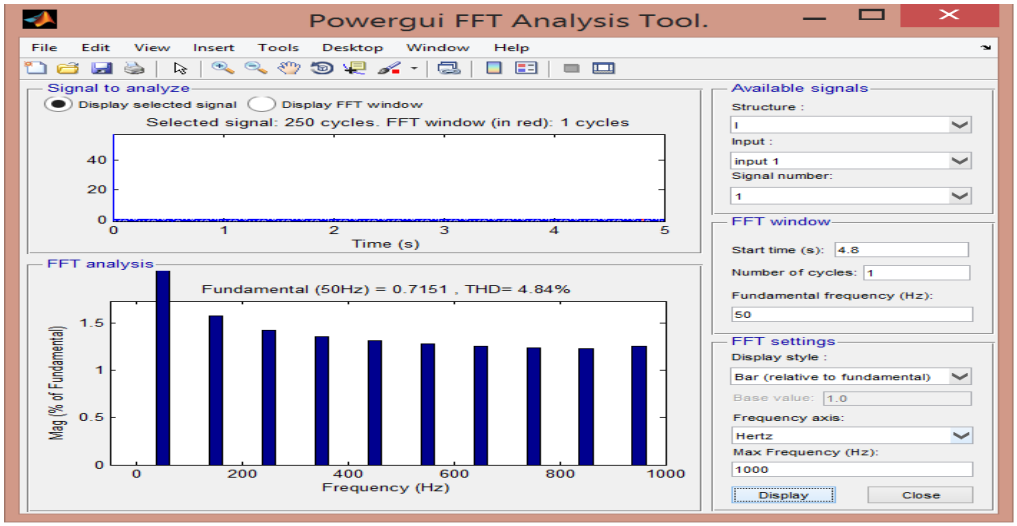

Fig 11. FFT analysis of the modified SEPIC converter with harmonic reduction technique.

The harmonic distortions were reduced to 4.8% when an operating voltage of 127Vrms is given at the input side and the power factor of the total system was improved to 0.96. As the harmonics are reduced the power factor of the system is improved. Because of the improved power factor the efficiency of the overall system was increased to 96%. Input voltage given to the converter is 187V and the converter produces an output voltage of 400V. The duty ratio is equal to 0.38 with a switching frequency of 30KHz. When an input voltage of 220Vrms is given the power factor gets improved to 0.988 and the harmonic distortions get reduced from 35% to 8% but simulation is not shown.

V. CONCLUSION

The power factor correction shapes the input current of off-line power supplies to maximize the real power available from the mains. Ideally, the electrical appliance should present a load that includes a pure resistor, so that the reactive power drawn by the device is zero. The input current harmonics are absent, the input current is a perfect replica of input voltage (sine wave). The current drawn from the mains is at a minimum for the real power required to perform the needed work, and this minimises losses and cost associated. The freedom from harmonics also minimizes interference with other devices being powered from the same source.

The experimental results presented operating with the third harmonic reduction technique shows that the total input current harmonic distortion is reduced from 13%to5.3% operating with an input voltage equal 127 V_{rms} and is reduced from 35.9% to 8.84% operating with an input voltage equal to 220 V_{rms}, considering a total input voltage harmonic distortion equal to 3.1%. The power factor is higher than 0.988 with the third harmonic reduction in all input voltage range. The efficiency operating with input voltage equal to 127 V_{rms} and output power equal to 108 W is equal to 95.6%. The experimental results show that there is also an increment in the converter efficiency operating with the third-harmonic reduction modulation that mainly occurs at light load operation in 127 and 220 V_{rms}.

ACKNOWLEDGMENT

I take this opportunity to convey my deep and sincere thanks to my respectable guide Dr Priya G Das for her valuable help and providing necessary facilities to make this work a successful one.

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