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Conditional Capturing System for Low Power Clock Distribution Networks

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***Abstract*—*Low-power design is becoming a crucial design objective due to the growing demand on portable applications and increasing difficulties in cooling and heat removal. A clock distribution network (CDN) delivers the clock signal which act as a reference to all sequential elements in the synchronous systems. The clock distribution network consumes a considerable amount of power in electronic devices. The proposed conditional capturing method for clock distribution using current is used to distribute a global clock. Further a pulsed logic is adapted to reduce the power consumption. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals. When the CMPFFE is combined with pulsed logic, the design results in lower average power compared to traditional voltage mode clocks*.

***Keywords*—** *CMPFFE, current mode, low power clock distribution, pulse logic, skew*.

I. INTRODUCTION

Low Power VLSI

The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before. Requirements for lower power consumption continue to increase significantly as components become battery-powered, smaller and require more functionality. In the past the major concerns for the VLSI designers was area, performance and cost. Power consideration was the secondary concerned. Now a day's power is the primary concerned due to the remarkable growth and success in the field of personal computing devices and wireless communication system.

Clock Distribution Network

The clock distribution network in digital integrated circuits distributes the clock signal which acts as a timing reference controlling data flow within the system. Since the clock signal has highest capacitance and operates at high frequencies, the clock distribution network consumes a large amount of total power in synchronous system. The main objectives in the design of CDNs are to minimize skew, jitter, and power. Clock skew is defined as the difference in the arrival time of the clock edges at different locations in the CDN. Skew is mainly caused by variations between clock buffers, interconnect widths, and loading at different clock paths. Clock jitter is defined as the difference in the arrival time of the clock edge at the same location in the CDN.

Clock Distribution Network Structures

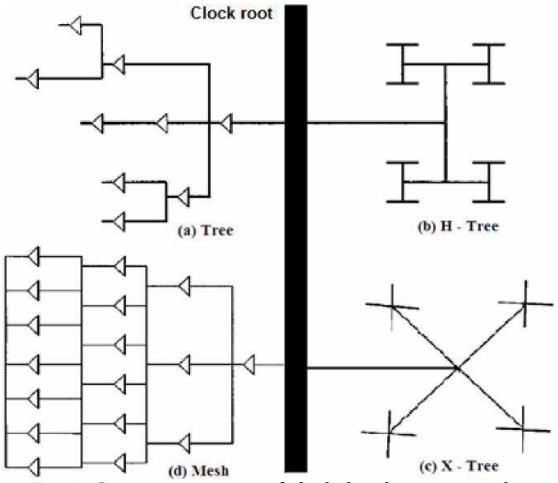

Fig. 1. Common structures of clock distribution networks

II. RELATED WORKS

A various papers which are essential to know the previously available techniques and their significance and limitations. These papers describe various methods to increase the throughput. The area and power consumption overhead coming from these methods are discussed here

Riadul Islam and Matthew R. Guthaus, " Low-Power Clock Distribution Using a Current-Pulsed Clocked Flip-Flop", IEEE transactions on circuits and systems-I: regular papers, vol. 62, no. 4, April 2015[9]. In this paper the implemented CDN network that uses current instead of voltage. The high performance current mode pulsed flip flop with enable (CMPFFE) is combined with the CM transmitter. It is also used for the one to many clock distribution networks. CDN exhibits 62% lower average power. The CMPFFE uses an input current-comparator (CC) stage, a register stage, and a static storage cell. The CC stage compares the in put push pull current with a reference current and conditionally amplifies the clock to a full-swing voltage pulse that triggers the data to latch at the register stage. If the resistance of wire to high means, it will affect the performance of the CMPFFEs.

Riadul Islam, Matthew R. Guthaus, "Current-mode clock distribution" in Proc.ISCAS, Jun. 2014, pp. 1203–1206[10]. In this paper the clock distribution that use current rather than voltage .One to many clock distribution network is used. To accomplish this, a new high-performance current-mode pulsed flip-flop (CMPFF) using 45 nm CMOS technology. The high performance current mode pulsed flip flop (CMPFF) is combined with the CM transmitter. In CMPFF method there is

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no enable signal is used. It consumes high power compared with clock distribution using a CMPFFE.

Byung-Do Yang "Low-power and area-efficient shift register using pulsed latches" IEEE transactions on circuits and systems—I: regular papers, vol. 62, no. 6, June 2015[2]. In this paper he proposes a low-power and area-efficient shift register using pulsed latches. The area and power consumption are reduced by replacing flip-flops with pulsed latches. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches. A master-slave flip-flop using two latches can be replaced by a pulsed latch consisting of a latch and a pulsed clock signal. All pulsed latches share the pulse generation circuit for the pulsed clock signal. As a result, the area and power consumption of the pulsed latch become almost half of those of the master-slave flip-flop. This shift register saves 37% area and 44% power compared to the conventional shift register with flip-flops.

M. Dave, M. Jain, S. Baghini, and D. Sharma, "A variation tolerant current-mode signaling scheme for on-chip interconnects," IEEE Trans.Very Large Scale Integr.(VLSI) Syst., vol. PP, no. 99, pp. 1–12, Jan.2012[6]. In this paper they propose a variation tolerant dynamic overdriving CMS scheme. Variation tolerant CM scheme including Rx and Tx circuits and the inverter amplifier Rx circuit provides low-impedance to ground and holds the terminal point at the switching threshold. However, this comes at the expense of large static and dynamic power when compared to the other CM techniques and makes it unattractive compared to existing VM signaling.

Y.-T. Hwang, J.-F. Lin, and M. hwa Sheu, "Low-power pulse-triggered flip-flop design with conditional pulse-enhancement scheme," IEEE Trans.Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 2, pp.361–366, Feb. 2012[11]. In this paper a novel low-power pulse-triggered flip-flop (FF) design is presented. A simple two-transistor and gate design is used to reduce the circuit complexity. Second, a conditional pulse-enhancement technique is devised to speed up the discharge along the critical path only when needed. As a result transistor sizes in delay inverter and pulse-generation circuit can be reduced for power saving. Maximum power saving against rival designs is up to 38.4%.

III. PROPOSED BLOCK DIAGRAM

The proposed block diagram for the conditional capturing system is shown in figure 2. The block diagram consists of a three blocks. There are current mode transmitter, current mode pulsed flip flop with enable and a pulsed latches.

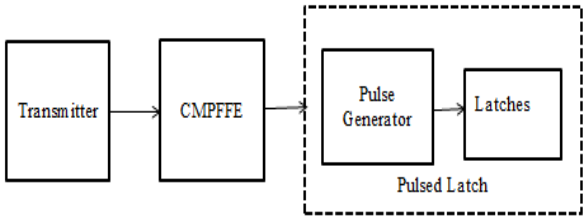

Fig. 2. Block diagram

IV. PULSE LOGIC

In a pulsed logic a latch synchronized by a pulse clock which is called pulsed latch. A pulsed latch can be approximated as a fast, lower power, and small FF. A pulsed latch consisting of a latch and a pulsed clock signal shown in figure 3. All pulsed latches share the pulse generation circuit for the pulsed clock signal. By using the pulsed latch the pulse distortion and clock skew can be well controlled. As a result, the area and power consumption of the pulsed latch become almost half. The pulsed latch is an attractive solution for small area and low power consumption.

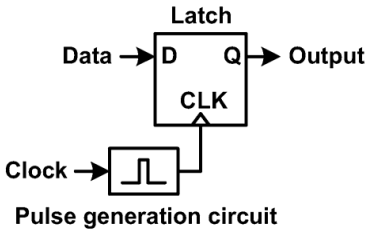

Fig. 3. Pulsed latch

In the conventional delayed pulsed clock circuits, the clock pulse width must be larger than the summation of the rising and falling times in all inverters in the delay circuits to keep the shape of the pulsed clock. However, in the delayed pulsed clock generator in figure 6 the clock pulsed width can be shorter than the summation of the rising and falling times because each sharp pulsed clock signal is generated from an AND gate and two delayed signals. Therefore, the delayed pulsed clock generator is suitable for short pulsed clock signals.

V. CURRENT MODE TRANSMITTER

In order to integrate the CMPFFE, a Tx provides a push pull current into the clock network and distributes the required amount of current to each CMPFFE. The Tx receives a traditional voltage CLK from a PLL/clock divider at the root of the H-tree network and supplies a pulsed current to the interconnect which is held at a near constant voltage. The clock distribution is a symmetric H-tree with equal impedances in each branch so that current is distributed equal to each CMPFFE leaf node.

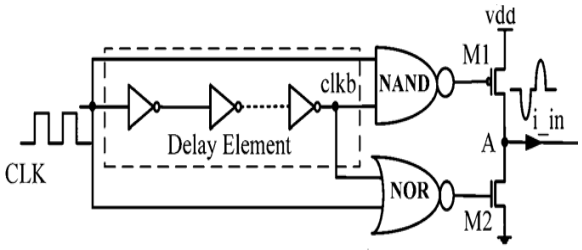

Fig. 4. Current mode transmitter

The pulsed current Tx is shown in figure 4. The NAND gate uses the CLK signal and a delayed inverted CLK signal, clkb, as inputs to generate a small negative pulse to briefly turn on M1. Hence, the PMOS transistor briefly sources charge from the supply while the NMOS is off. Similarly, the

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NOR gate utilizes the negative edge of the CLK and clkb signals to briefly turn on M2. Hence, the NMOS transistor briefly sinks current while the M1 is off. The non-overlapping input signals from the NAND-NOR gates remove any short circuit current from Tx.

VI. CMPFFE

The CMPFFE uses an input current-comparator (CC) stage, a register stage, and a static storage cell. The CC stage compares the input push pull current with a reference current and conditionally amplifies the clock to a full-swing voltage pulse that triggers the data to latch at the register stage. The feedback pulsed FF is in stark contrast to the previous CM schemes which utilized expensive Rx circuits and buffers to drive the final FFs.

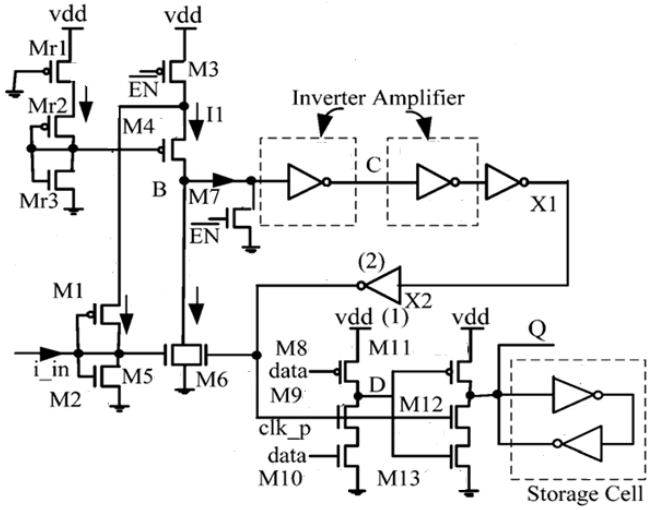

Fig. 5. CMPFFE

VII. PROPOSED SYSTEM

Conditional Capturing System

A conditional capturing system is a proposed system for the low power clock distribution networks. A conditional capturing system uses a current mode transmitter. The current mode pulsed flip flop with enable is used in the conditional capturing system enhancement. There is a pulsed logic technique is used to transmit the clock signal as a pulsed clock to get an output. In a pulsed logic a latch synchronized by a pulse clock which is called pulsed latch. A pulsed latch is consisting of a latch and a pulsed clock signal which is generated by a pulse generator. All pulsed latches share the pulse generation circuit for the pulsed clock signal.

Proposed Circuit Diagram

The figure 6 shows the proposed conditional capturing system's circuit diagram. The given input signal is transmitted through the transmitter circuit. The transmitter circuit is interconnected with the CMPFFE circuit.

The signal is amplified and transfer through the pulse generator circuit. And also the latch receives the amplified signal and gives the output with reduced skew rate. By using this circuit the power is consumed in the clock distribution networks.

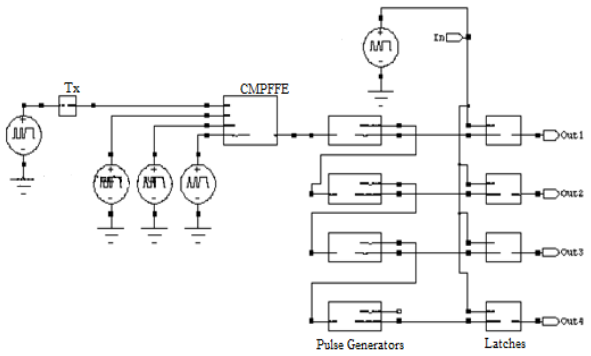

Fig. 6. Proposed circuit diagram

Schematic View

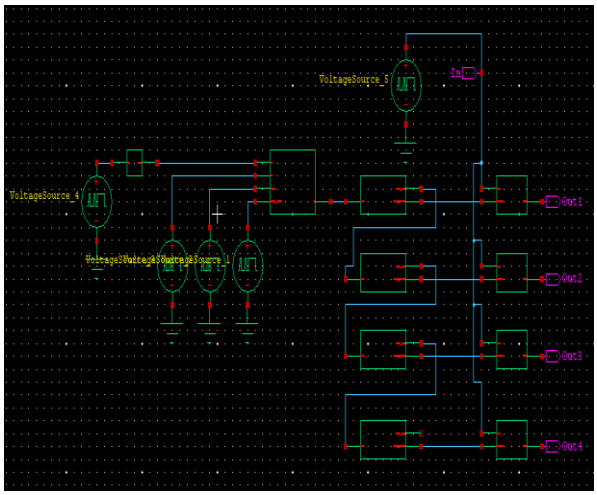

Fig. 7. S-Edit window showing the schematic view

The figure 7 shows that the S-Edit window of the conditional capturing system.

Output Waveform

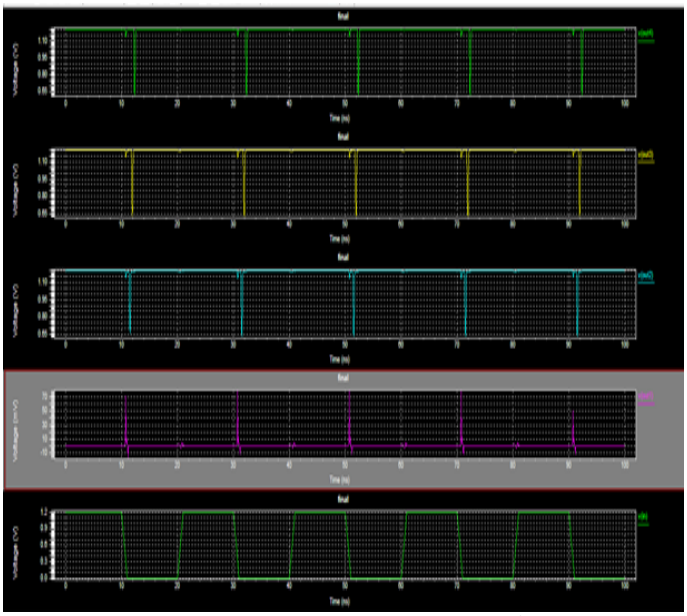

Fig. 8. W-Edit window showing output wave form

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In figure 8 the W-Edit window showing the output wave forms of the proposed system. In the wave form analysis the input wave form is transmitted through the pulsed latch and gives the clock signal as the pulses.

VIII. CONCLUSION

By using the pulsed logic technique the conditional capturing system is designed and simulated which is used in the Clock Distribution Networks (CDNs). The power consumption result of the conditional capturing system is compared with the existing system. The power consumption is reduced and the clock signal is amplified with reduced skew rate. The designs are designed and simulated by using the Tanner EDA tool.

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