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Correction of Multiple Errors with Seamless Pipeline Operation Using AHL

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***Abstract*—** *A low power flip-flop (FF) design featuring an explicit type-pulsed triggered structure and a modified true signal phase clock latch based on a signal feed through scheme is presented. The proposed design successfully solves the long discharging path problem in seamless pipeline operation and achieves better speed and power performance. If error will be happen in any received data, the entire clock will be stop because of razor based shadow latch flip-flop skip the entire portions. So, I had to add AHL a keeper technique. Here I designed the circuit as error occurred at the pipeline is transferred to AHL it contains some process to clear the error and continue to the pipeline.*

***Keywords*—** *Error correction, razor flip flop, AHL.*

I. INTRODUCTION

Very Large Scale integration is the process of creating an integrated circuit by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. Before the introduction of VLSI technology most ICs had a limited set of functions they could perform. An electronic circuit might consist of a CPU, ROM, RAM and other glue logic. VLSI lets IC makers add all of these into one chip.

A. Testing of VLSI Chip

Testing of VLSI chip is becoming very much complex day by day due to increasing exponential advancement of Nano technology. A low power flip-flop is a design technique that allows a system to test automatically itself with slightly larger system size. Testing of system is an experiment in which the system is exercised and its resulting response is analyzed to ascertain whether it behave correctly. In this paper, the simulation result performance achieved by D- latch and pulse triggered flip-flop through Tanner this is enough to compensate the extra hardware needed in pipeline operation. This technique generates solution for the long discharging path problem, so it can provide seamless pipeline operation without any error and also to achieve better speed and power performance.

B. Gate Delay

Transistors within a gate take a finite amount of time to switch. This means that a change on the input of a gate takes a finite amount of time to cause a change on the output. This time is known as Propagation Delay. Smaller transistors mean faster switching times. Semiconductor companies are continually finding new ways to make transistors smaller, which means transistors are faster, and more can fit on a die in the same area.

II. LITERATURE SURVEY

A various papers which are essential to know the previously available techniques and their significance and limitations. These papers describe various methods to increase the throughput. The area and power consumption overhead coming from these methods are discussed here.

Insup Shin Jae-Joon Kim and Young Soo Shin, Aggressive Voltage Scaling Through Fast Correction of Multiple Errors With Seamless Pipeline Operation, IEEE transactions on circuits and systems I: regular papers, vol. 62, no. 2, February 2015 [1]. Aggressive reduction of timing margins, called timing Speculation, is an effective way of reducing the supply voltage for a pipeline circuit and thereby its power consumption. However, probability of timing error increases with the voltage scaling and hence, the errors must be corrected with small cycle penalty. We introduce an improved Razor flip-flop which makes more effective use of its shadow latch, so that a pipeline stage can correct an error while continuing to receive data. This avoids the need for repeated clock gating when timing errors happen simultaneously at different stages, or when an error persists. The new flip-flop also facilitates time-borrowing. Our technique uses less energy than the state-of-the art technique, and the energy saving increases with pipeline length: with 10 stages, 4–9% smaller energy is used.

I-Chyn Wey, Chien-Chang Peng, and Feng-Yu Liao, "Reliable Low-Power Multiplier Design Using Fixed-Width Replica Redundancy Block", IEEE transactions on very large scale integration (VLSI) systems, vol. 23, no. 1, January 2015 [7]. In this paper, we propose a reliable low-power multiplier design by adopting algorithmic noise tolerant (ANT) architecture with the fixed-width multiplier to build the reduced precision replica redundancy block (RPR). The proposed ANT architecture can meet the demand of high precision, low power consumption, and area efficiency. We design the fixed-width RPR with error compensation circuit via analyzing of probability and statistics. Using the partial product terms of input correction vector and minor input correction vector to lower the truncation errors, the hardware complexity of error compensation circuit can be simplified. In a 12 × 12 bit ANT multiplier, circuit area in our fixed-width RPR can be lowered by 44.55% and power consumption in our ANT design can be saved by 23% as compared with the state-of-art ANT design.

S. Meena and I. Rabeek Raja, "Correction of multiple errors with seamless pipeline operation using AHL," *International Research Journal of Advanced Engineering and Science*, Volume 1, Issue 2, pp. 131-134, 2016.

I. Shin et al., "Power minimization of pipeline architecture through 1-cycle error correction and voltage scaling," in Proc. ASPDAC, Jan.2014, pp. 179–184 [3]. We present a new 1-cycle timing error correction method, which enables aggressive voltage scaling in a pipelined architecture. The proposed method differs from the state of the art in that the pipeline stage where the timing error occurs can continue to receive input data without halting to avoid data collision. The feature allows the pipeline to avoid recurring clock gating when timing errors happen at multiple stages or timing errors continue to occur at a certain stage. Compared to a state of the art method, the proposed method shows 2-6% energy reduction for a 5-stage pipeline and 7-11% reduction for a 10-stage pipeline. In addition, the proposed logic to propagate clock gating signal is much simpler than that of the previous method by eliminating reverse propagation path of clock gating signal.

Insup Shin, Jae-Joon Kim, Yu-Shiang Lin, Youngsoo Shin. "A pipeline architecture with 1-cycle timing error correction for low voltage operations," in Proc. ISLPED, Sep. 2013, pp. 199–204 [4]. We present a new timing error correction scheme which allows each pipeline stage to halt for one cycle only. The small timing penalty for the error correction operation in the proposed scheme makes it possible to eliminate the extra timing guard band that was needed to accommodate timing uncertainty due to process variations. As a result, lower supply voltage can be used with the proposed scheme for low power operations. Compared to the previous 1-cycle error correction scheme which uses two-phase transparent latch based pipeline, the proposed scheme can be applied to the pipeline based on more popular clocking elements such as flip-flop or pulsed latch.

Y. Liu et al., "On logic synthesis for timing speculation," in Proc. ICCAD, Nov. 2012, pp. 591–596 [8]. K. A. Bowman et al., "Energy-efficient and metastability immune resilient circuits for dynamic variation tolerance," IEEE J. Solid-State Circuits, vol. 44, no. 1, pp. 49–63, Jan. 2009 [9], by allowing the occurrence of infrequent timing errors and correcting them with rollback mechanisms, the so called timing speculation (TS) technique can significantly improve circuit energy-efficiency and hence has become one of the most promising solutions to mitigate the ever increasing variation effects in nanometer technologies. As timing error recovery incurs non-trivial performance/energy overhead, it is important to reshape the delay distribution of critical paths in timing speculated circuits to minimize their timing error rates. Most existing optimization techniques achieve this objective with post-synthesis techniques such as gate sizing or body biasing. In this work, we propose to conduct logic synthesis for timing-speculated circuits from the ground up.

III. Related Work

A. RFF

To modify the clock signal sent to the shadow latch in such a way that the shadow latch opens after the main flip-flop has captured its input data. Then the shadow latch can restore the previous, and correct, data to the main flip-flop to achieve error correction, while also capturing new input data in the same cycle. This avoids the data conflict.

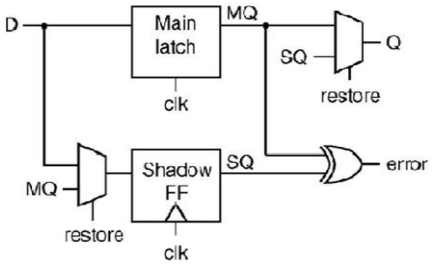

Fig. 1. Razor flip-flop

If any flip-flop in a stage receives a signal with critical path delay, then all the flip-flops in that stage must be replaced by RFFs. This is because shadow latch is used for error correction, as well as capturing data during error correction. While many flip-flops are on a critical path, a much smaller proportion has critical paths both starting from and terminating at them. This motivates us to exchange the positions of the flip-flop and latch in an RFF, so as to allow time borrowing, which can reduce the error-rate. When a latch is moved on to a data path, the extent of the hold-time violation that it brings is the same as that introduced by a flip-flop. It tunes the supply voltage by monitoring the error rate during operation. It monitors both global and local delay variations. It uses shadow latch to flush the errors in pipeline operation and execute the data again after correction.

B. AHL

AHL refers to Adaptive Hold Logic. Here the Adaptive Hold Logic is act as a keeper technique. It just holds the error and start the process in feedback type. It contains aging indicator for that it designed with counter, comparator and gating circuits.

The counter will counts the error occurred in pipeline stage, it is a up counter. Then the counter value is compared with comparator circuit which has threshold value as 2. When it attains more than 2 count of error, it automatically gating get disable and send these error data and the gating circuit gets enable. It acts as a feedback circuit

IV. Proposed Work

To require the fastest possible mechanism for error correction introduced one-cycle error correction for flip-flop and pulsed-latch designs, but the technique cannot handle a massive number of simultaneous errors. The contribution of this paper is a new method of one cycle error correction which is capable of reducing the overall timing penalty for the correction of large numbers of errors which occur at the critical operating voltage. In RFF it skip the error and have a continue process and so we unable to receive the complete signal. To overcome this i use Adaptive Hold Logic in combination of Razor flip-flop and to maintain delay period the AHL acts as a feedback circuit. If error occurs in an any received data it stored in shadow latch and maintain the count using counter.

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Here I kept the threshold value of 2 to compare the counter value if counter exceeds the threshold value the gating logic in AHL will disable. After finishing the process of error data automatically the gating gets enable and the pipeline process is continued.

A. Counter

The 2 – bit counter circuit with D- flip flop is used here it will count the error data occurred in pipeline operation. It just count the error occurrence.

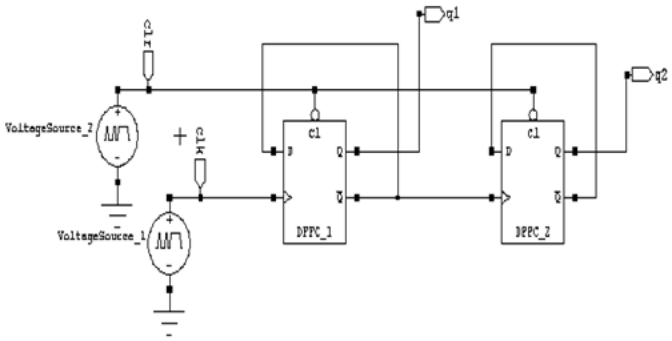

Fig. 2. Counter circuit

B. Comparator

The comparator circuit will compare the error counted using counter circuit with the threshold value. Here I fix the threshold value as 2. When the error count is exeed 2 the gate will closed.

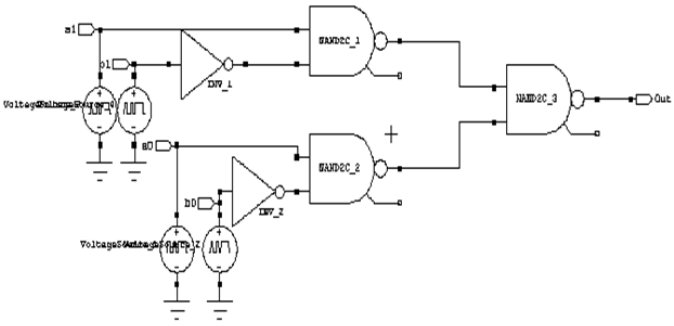

Fig. 3. Comparator circuit

C. Circuit Diagram

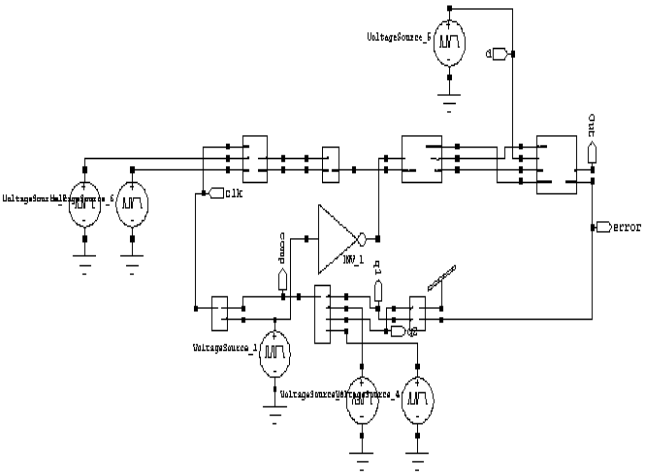

Fig. 4. Circuit diagram

It is the circuit diagram of the proposed methodology, where the circuits designed for the Adaptive Hold Logic are converted into symbols. And it is called back to the design at the time of simulating. The input bits are given through voltage source

D. Schematic View

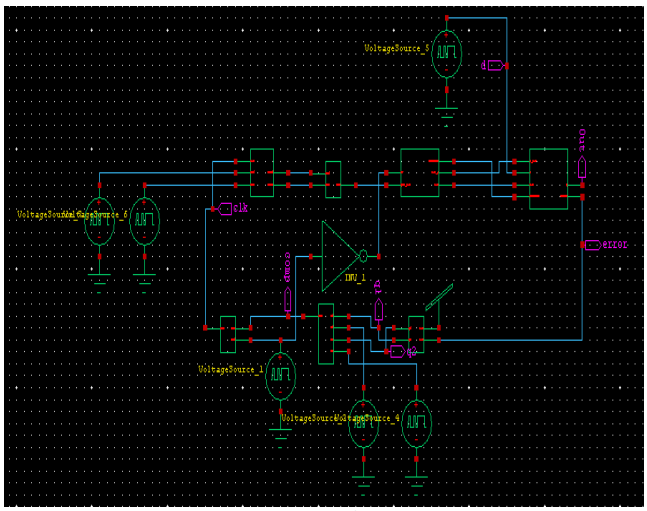

Fig. 5. Schematic view of proposed method

The schematic is designed using Tanner EDA tool. Here I used version 13. In this schematic diagram the RFF is combined with AHL and provide the pipelined data. Here it designed by assigning the error occurred at pipeline and it corrected through feedback circuit. The output of each stage is viewed in output waveform. The T-Spice is coded and the output waveform is generated.

E. Output Waveform

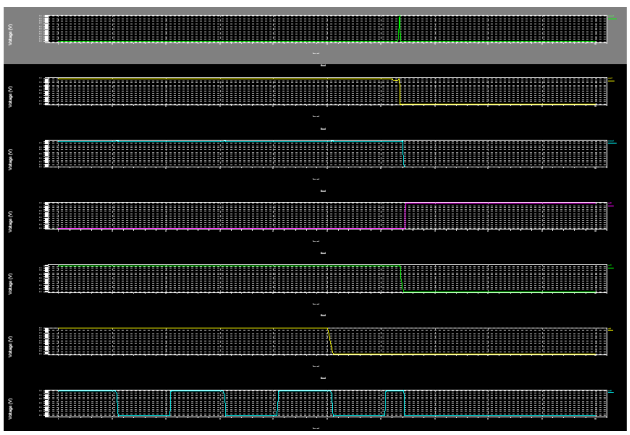

Fig. 6. Final output waveform

F. Power Analysis

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* BEGIN NON-GRAPHICAL DATA

Power Results
vi from time 0 to 1e-007
Average power consumed -> 2.151087e-003 watts
Max power 5.947249e-003 at time 1.50819e-008
Min power 4.994622e-004 at time 8.07926e-008
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Fig. 7. Power

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The power analysis of the entire circuit is calculated. The maximum and minimum power also calculated using power calculator.

G. RFF

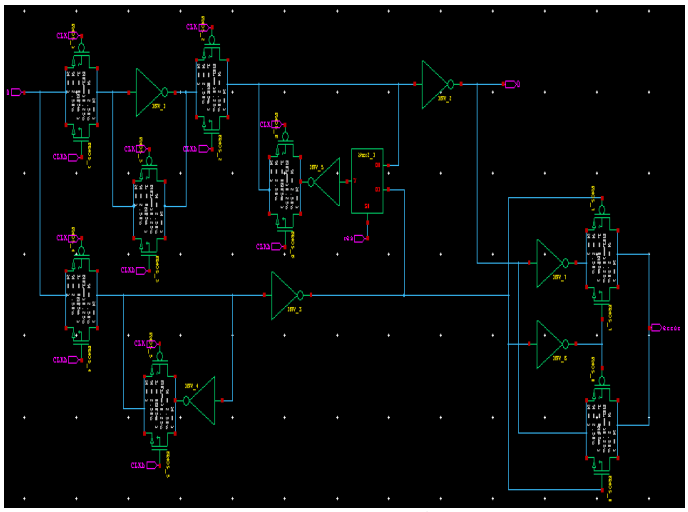

Fig. 7. Schematic view of RFF

H. Waveform

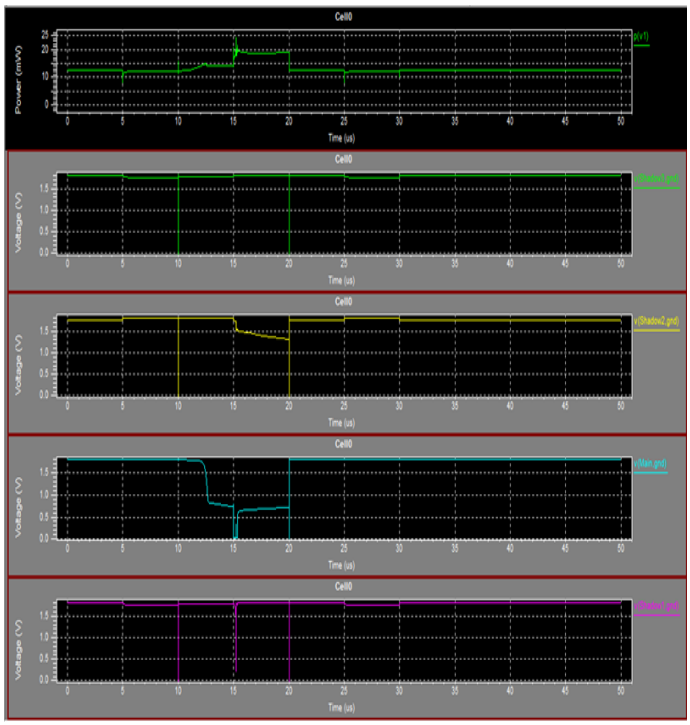

Fig. 6. Output waveform of RFF

V. CONCLUSION

In this paper, a low power RFF with D- Latch design is presented. The proposed circuit is implemented in 90nm process. The continuous signal is passed through pipeline. The delay error is corrected in respective stages, if it continues to stage four with error then it feed back to the second stage and continues the pipeline process without error. So these methods need more area for sequential logic than counter flow pipelining.

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