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Gate All Around (GAA) FET Modeling Using 2D Material as Channel

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Abstract— *Gate All Around (GAA) field effect transistor (FET) is a semiconductor device used in many electronic devices for amplification and switching electrical signals. FET downscaling has been the driving force towards the technological advancement, but continuous scaling down of FET causes problem of high power dissipation, high leakage current, Short Channel Effects (SCEs), excessive process variations and reliability issues. The purpose of this research work is to describe the modeling of the performance of 2D material such as (WSe2, MoSe2, etc.,) nanowire GAA FETs and to study their performance as parameter of the transistor's structure variation like diameter, gate dielectric thickness, and gate dielectric constant. Simulations of ballistic transport in the calculation of the current-voltage (I-V) characteristics for nanoscale double gate FETs. GAA FET channel lengths are getting smaller and high-mobility channel materials are being used, near-ballistic models of MOSFET device physics operation is being realized.*

Keywords— *GAA, Channel, Nanowire, FET.*

I. INTRODUCTION

One of the most important aspects of modern nanoelectronic research is to scale down devices [1]. Scaling down device comes along with issues as in case of MOSFET channel lengths continue to shrink upto few nanometer, but it counter the performance degradation and causes short channel length problems [2]. In order to overcome, two dimensional (2D) nanomaterials have been introduced as these nanomaterials because of their exotic electrical, novel chemical, optical and rich physics properties [3]. 2D materials include graphene, hexagonal boron nitride (h-BN), metal dichalcogenides, metal trichalcogenides, black phosphorous, metal oxides, MXenes (silicene, germanene, etc.), metal hallides, and metal carbides [3].The first well-known 2D material is graphene (Gr)[2], and is first studies as the channel material for fast field effect transistors[4], because of its excellent carrier mobility (up to ~105 cm2 V−1 s−1) and micrometer electron mean free path[5] .Gr is also called as a wonder material due to its 2D honeycomb lattice [6] .Gr can be produced either by top-down or bottom-up approaches. In top-down approach, Gr is usually synthesized via electrochemical, mechanical, and chemical exfoliation of graphite, whereas the bottom-up approach uses chemical vapor deposition and chemical synthesis to produce grapheme. The family members of Gr have been used in nanoelectronics, energy storage, biosensing, catalysis, nanocomposites, and pharmaceuticals [7]. There occurs limitation of Gr i.e. it has gapless band structure which is not suitable for switching devices [8]. In order to overcome this disadvantage, new routes and solutions have been explored. Thus it was by replacing Gr as the channel material in lateral FETs with semiconducting 2D materials, such as [9] TMDCs, because of the new properties and applications that makes them a great contender for flexible electronic/optoelectronic device applications [10] or phosphorene (a 2D lattice composed of phosphorus atoms) [11]. TMDC layers are arranged in a hexagonal lattice and have attracted attention due to their pristine interfaces (without out-of-plane dangling bonds), thermal stability, and high scalability in device application [14]. TMDCs ($MoSe_2$, $MoTe_2$, WS_2, and WSe_2, etc.) are layered materials with sizable bandgap, transition from bulk to layered form (indirect to direct transition), resulting in unique physical properties expected to be employed in future semiconducting devices [15]. Typically, atomically layered TMDCs, such as molybdenum disulfide (MoS_2) and tungsten diselenide (WSe_2), are widely studied as attractive materials for enabling new nanoelectronic and optoelectronic device applications [16]. But back-gated WSe2 monolayer FETs with surface doping have already demonstrated a high field-effect mobility reaching ~140 cm2 V−1 s−1, that is substantially higher than most of the reported room temperature mobility values for MoS_2[18]. The VBM of WSe_2 is 0.46eV, while for MoS_2 is 1.5eV that make WSe_2 a promising candidate for spintronics applications [19]. Moreover under tensile strain, monolayer WSe_2 remains a direct bandgap material with a bandgap decrease rate of ~8 meV/% and multilayer WSe_2 undergoes an indirect to direct bandgap transition [20]. As the strain induced bandgap change will influence the resistivity of 2D materials [21], the smaller rate of bandgap change under strain of 2D WSe_2 [22]. Compared to MoS_2, WSe_2 has smaller electron/hole effective mass and thus higher mobility.

Nanowire FETs are important because they are potentially useful in low-power applications, have high packing densities, maintain high gate sensitivity, are capable of individual or bulk (arrayed)fabrication, are scalable, and have recently been investigated for ballistic carrier transport behavior for potential high-performance electronic devices [7]. Nanowire FETs even allow for bandgap engineering of the FET channel allowing designers to maximize device performance [8].There are several factors to consider when optimizing a FET device. Some of these include: low threshold voltage, high carrier mobility/speed, low leakage current, low power operation, low drive voltage operation, low series resistance, high transconductance (gate sensitivity), and good subthreshold characteristics.

According to the theory of ballistic nanotransistors [6], a non-equilibrium mobile charge is induced between the source and the drain if electric field is applied. The positive charge densities in source, negative charge densities in drain and

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equilibrium charge densities are related to the density of states and Fermi-Dirac probability distribution. The induced drain current can be determined by [15].

$$I_{DS} = \frac{2qkT}{\pi h}\left[F_0\left(\frac{U_{SF}}{kT}\right) - F_0\left(\frac{U_{DF}}{kT}\right)\right]$$

Here, $F0$ is the Fermi integral of order zero, k is the Boltzmann constant, ħ is the reduced Planck constant, T is the temperature, U_{SF} and U_{DF} are the potentials induced by terminal voltages at source and drain respectively as defined by

$$U_{SF} = E_F - qV_{SC}$$

$$U_{DF} = E_F - qV_{SC} - qV_{DS}$$

Where EF is the Fermi level, VSC is the self-consistent potential and VDS is the induced voltage between drain and source [20].

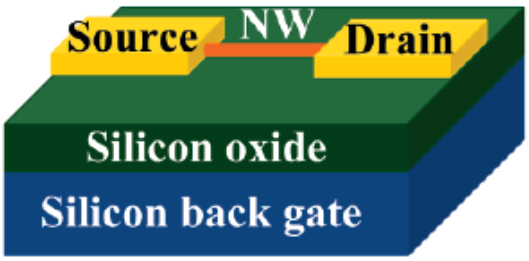

Fig. 1. Nanowire FET.

II. Simulation Approach

High mobility channel materials are being used as to realize low channel length dimension FET. Ballistic model of device physics is used to realize the operation the device. The modeling is proposed to achieve through FETToy tool [21]. The structure of the device is shown in Fig. 2. The channel material is the Tungsten Diselinide which is a 2D material. The simulation process flow is shown in Fig. 3. Research work is carried out to estimate the I-V characteristics of 2D nanowire based GGA FET. I-V and mobility profile of the device is studied from 10-50 nm diameter of the nanowire channel device.

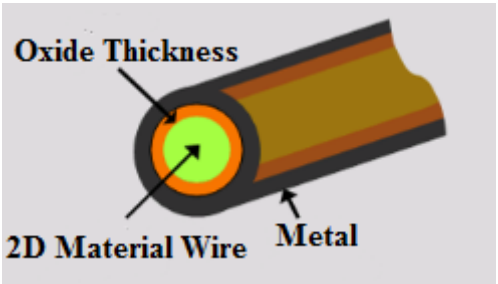

Fig. 2. Simulated device structure.

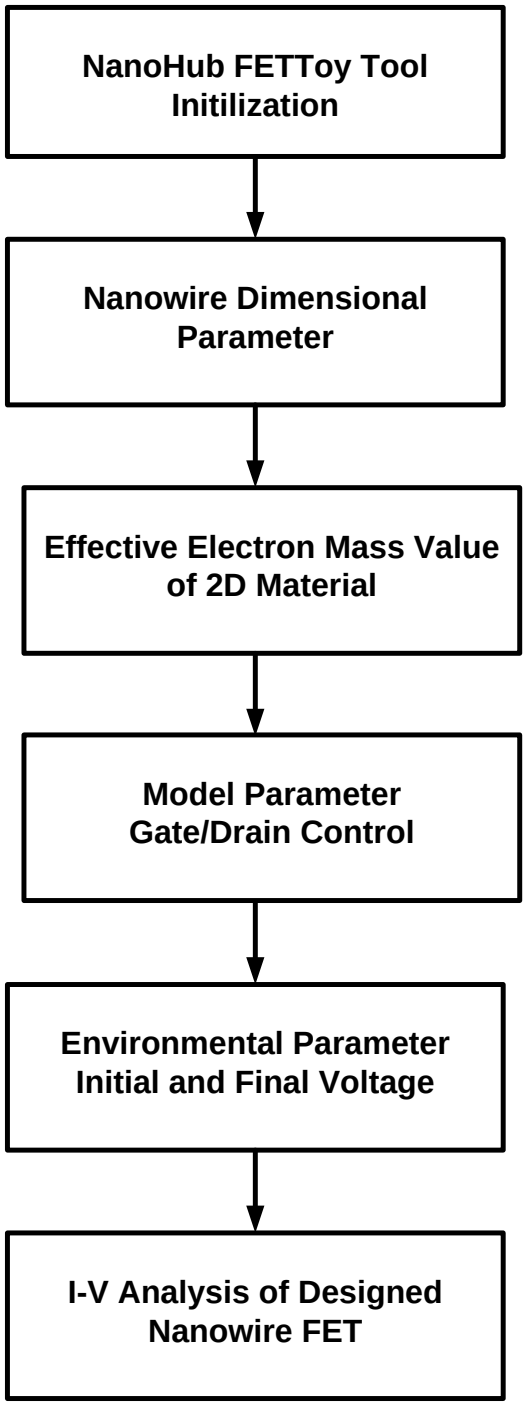

Fig. 3. Simulation process flow.

III. Results and Discussion

To optimize the performance of 2D material based device is presented by altering the device's structure and incorporates plots of the effects on device performance of variations in the FET structural parameters such as nanowire diameter. Plots are included of the current-voltage and mobility (e.g., Vd = 1.0V). We simulated the drain current-gate voltage characteristics for 10 nm to 50 nm with 10 nm step size

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nanowire diameters. Transfer characteristics of the device are simulated for 0-1V drain voltage with 13 step gate bias voltage from 0-1V and drain current was observed. Similarly mobility of the charge is also simulated from same range of drain voltage and bias voltage.

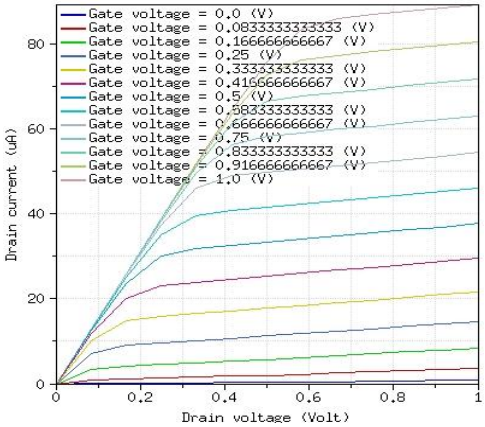

Fig. 4. I_d vs V_d characteristics of 10nm diameter with 13 point V_g biasing.

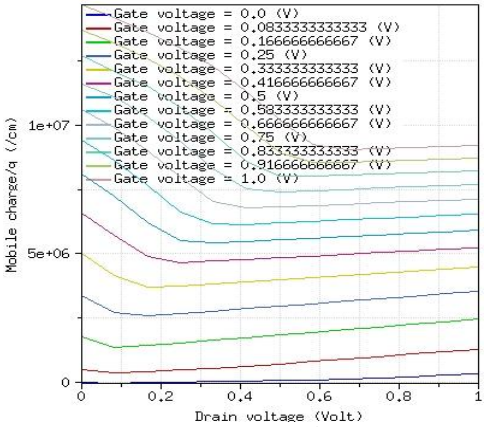

Fig. 5. Charge mobility vs V_d characteristics of 10nm diameter with 13 point V_g biasing.

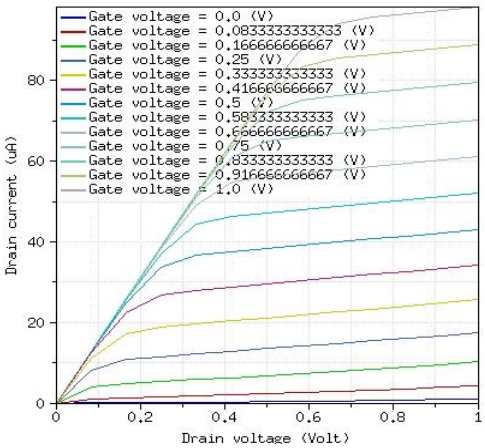

Fig. 6. I_d vs V_d characteristics of 20nm diameter with 13 point V_g biasing.

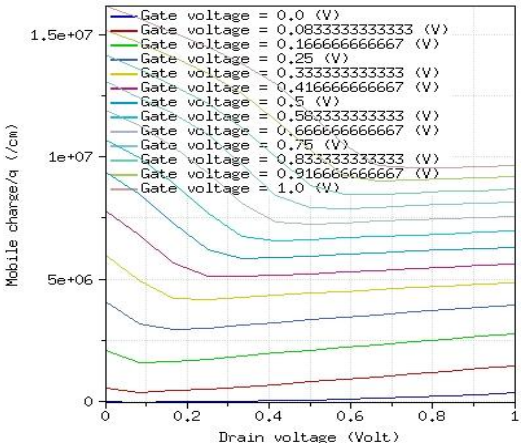

Fig. 7. Charge mobility vs V_d characteristics of 20nm diameter with 13 point V_g biasing.

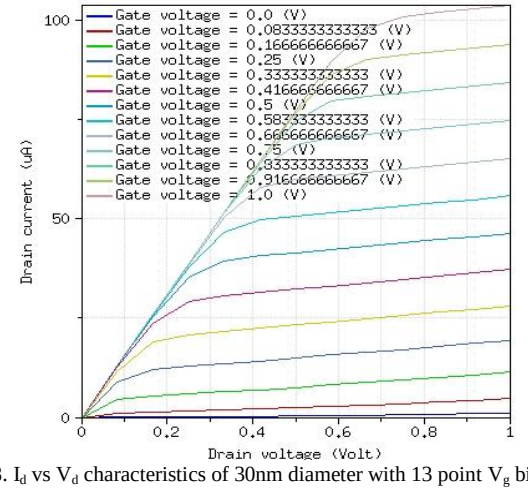

Fig. 8. I_d vs V_d characteristics of 30nm diameter with 13 point V_g biasing.

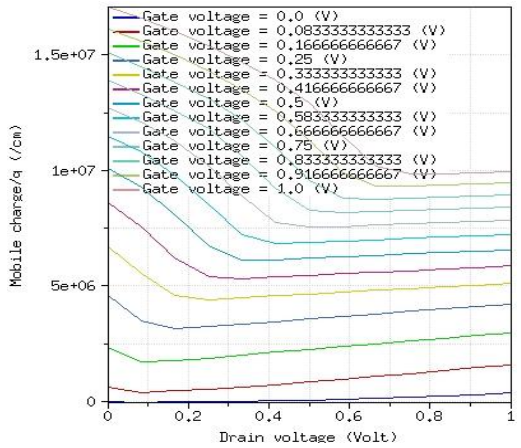

Fig. 9. Charge mobility vs V_d characteristics of 30nm diameter with 13 point V_g biasing.

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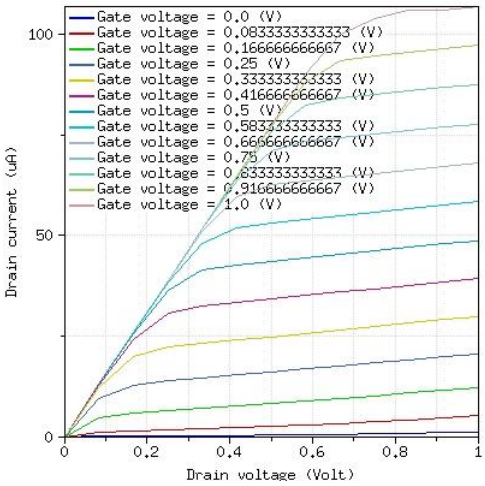

Fig. 10. I_d vs V_d characteristics of 40nm diameter with 13 point V_g biasing.

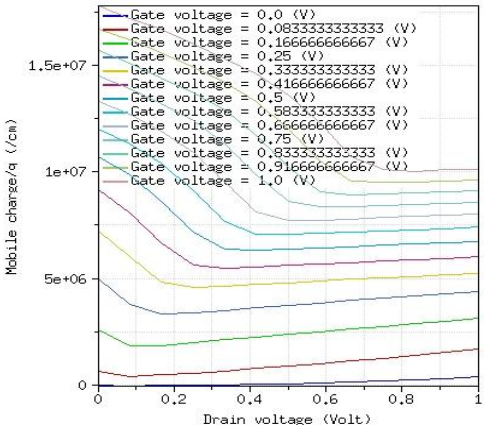

Fig. 11. Charge mobility vs V_d characteristics of 40nm diameter with 13 point V_g biasing.

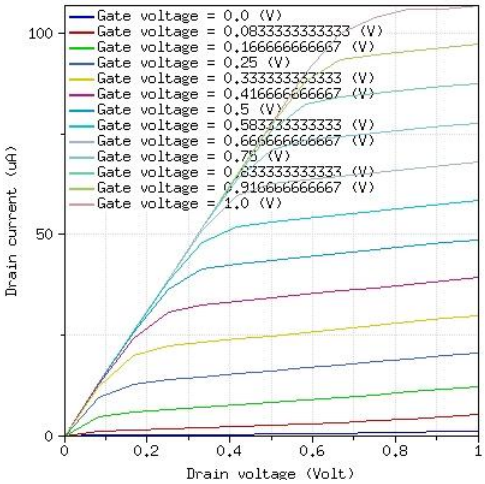

Fig. 12. I_d vs V_d characteristics of 50nm diameter with 13 point V_g biasing.

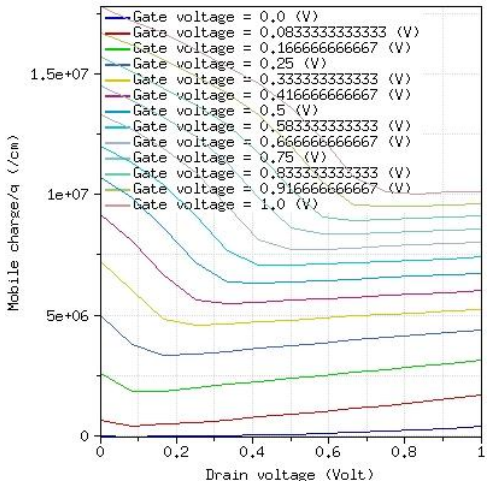

Fig. 13. Charge mobility vs V_d characteristics of 50nm diameter with 13 point V_g biasing

From the plot it is observed that with the increase dimensions (diameter of the channel) drain current gradually increases and attains saturation after 0.5 V drain voltage. It can be seen in transfer characteristics graph that maximum current for 10 nm, 20nm, 30nm, 40nm, and 50nm diameter channel is ~80uA, ~90uA, ~100uA, ~110uA, and ~110uA respectively. In case of mobility charge carries for 10nm diameter channel is lower as compared to other channel simulated in research work.

IV. Conclusion

In the research work gate all around (GAA) field effect transistor (FET) are simulated with 2D material (WSe_2) nanowires based channel. Diameter of the nanowires were considered from 10-50nm. It is observed from the simulated results that diameter of the nanowires is critical for active region of the device characteristics. Mobile charge carrier confinement occurs at low dimension nanowire in GAA FET device.

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