International Research Journal of Advanced Engineering and Science
ISSN (Online): 2455-9024

Design A Couple Inductor DC-DC Converter to Increase Conversion Ratio and Efficiency Using For Solar Energy System

Nguyen Chi Hung[1], Ngo Dinh Thanh[2]
[1]Sai Gon University, Ho Chi Minh City, 700000, Vietnam
[2]Mien Trung University of Civil Engineering, Tuy Hoa City, Phu Yen Province, 560000, Vietnam

Abstract *– This paper introduce a new step-up DC-DC converter with high step-up conversion ratio. DC analysis is presented and the static characteristics are expected to show that the static conversion ratio exhibits a high voltage boost, the converter still stable operating at narrow cycle duty. The proposed converter ratio at the same duty cycle D is (1+nD) time higher than the classical Boost, where n is the transformer ratio. Compared to quadratic converters the proposed topology has also one transistor and three diodes, but it eliminates two reactive elements. The converter is simulated and real tested on the physical couple inductor DC-DC converter designed and made. The simulation and the theory perfectly match. This new DC-DC converter could be a simple cheap solution in applications for rooftop solar energy systems.*

Keywords *– Boost converter; dc-dc conversion; static step-up conversion ratio.*

I. Introduction

One of the basic researches on DC-DC boost converter was conducted by Erickson's authors [1]. This is the initial research for the boost converter. It is very basic and primitive. The higher step-up ratio is, the lower the stability is, so that the scope of adjustment of the step-up ratio is very limited and effective extremely low output.

The team led by Ioiovici [2] built a hybrid DC-DC converter, with a wider range of variable ratio adjustment than Ericson's DC-DC. However, it is complicated, using many components, but the efficiency is not high, the step-up ratio is low and reverse bias applied to the semiconductor components is high, leading to large losses.

Pop-Cămlimanu et al. [3] developed the model of Ioiovici's author group [2], using the new hybrid Hybrid New-Boost Boost-L with less components, simpler topology, but efficiency and step-up conversion ratio is still low, the reverse voltage applied to the semiconductor components is still high and so the losses are still great.

All of the above models can only improve one of the DC-DC boost converter criteria, either too simple, or the scope to adjust a wider variable ratio, or a higher variable ratio, or high efficiencies without compromise and achieving the many criteria that in a DC-DC booster needs.

Therefore, this paper wants to design a DC-DC booster that uses coupled inductor to improve the efficiency and step-up conversion ratio of the solar system abbreviated by CIDCC. Solution is based on Ioiovici model.

II. Computing and Designing

2.1. Computing

Coupled Inductor Boost circuit (CIB) was developed based on the idea to increase the step-up conversion ratio of output compared to traditional boost circuits. The first step in the research and development of this new boost technology is to couple coils together to form an ideal transformer and analyze the converter's operation. From such analysis and comparison, it can be remarked that the ratio when using 2 inductors is significantly higher than when using one inductor in the basic boost circuit and the D4 diode is always disconnected. Now we will get a simple boost circuit but still effective as shown in Figure 2. The boost circuit now includes only 1 active switch, 3 passive switches, combined with one output capacitor and 2 inductors.

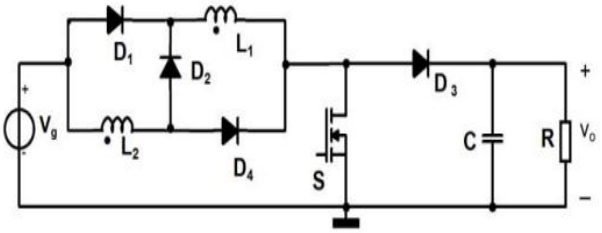

Figure 1: Coupled Inductor Boost Circuit

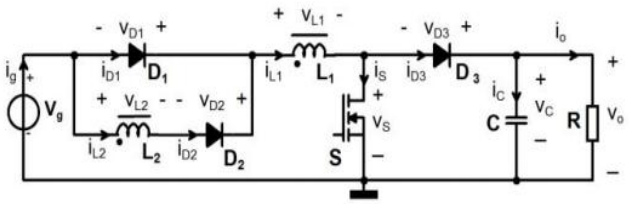

Figure 2: Proposed Coupled Inductor Boost Circuit

In the circuit above, there is 1 active switch, which is MOSFET, 3 passive switches, 3 diodes, output capacitor, and 2 coupled inductors with different turns, see Figure 2.

The circuit is controlled by continuous conduction mode (CCM) for diodes D1, D2, D3. Principles of CCM operation, the assumption of small ripple state variables is considered [5]-[7] during the analysis ideal operation.

There will be two states of the coupled inductor boost circuit, as the switch is closed and the switch is open. At this time the switching frequency of the switch will be denoted as fs and correspond to the switching period Ts. The converter is

Nguyen Chi Hung and Ngo Dinh Thanh, "Design A Couple Inductor DC-DC Converter to Increase Conversion Ratio and Efficiency Using For Solar Energy System," *International Research Journal of Advanced Engineering and Science*, Volume 5, Issue 2, pp. 167-172, 2020.

International Research Journal of Advanced Engineering and Science
ISSN (Online): 2455-9024

controlled by the PWM pulse width modulation method and the cycle is D.

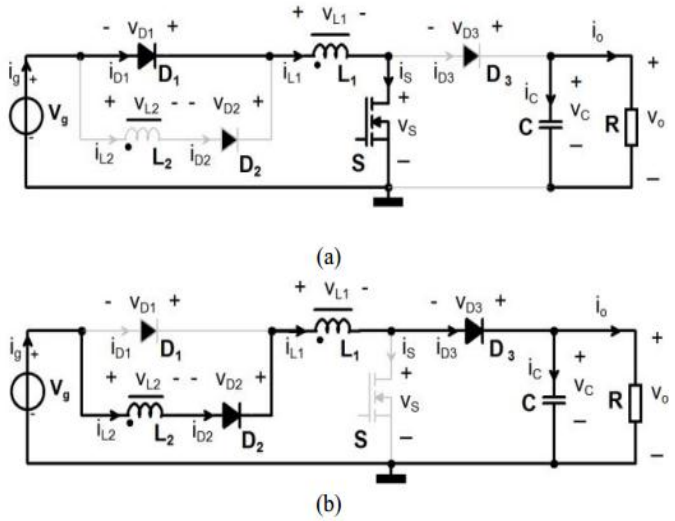

Figure 3: The two operating states of the CIB circuit in CCM

Fig. 3(a) shows the first operation state, from 0 to D·Ts, when transistor S and diode D1 are on, whereas diodes D2 and D3 are off due to reverse bias. The circuit is separated in two loops: the first has the voltage source Vg, the inductor L1 and returns to the ground of the voltage source. The second one includes the output capacitor C that is discharged to the resistance load R.

In the second operation state, Fig. 3(b), from D·Ts to Ts, when transistor S and diode D1 are off, diodes D2 and D3 are on. The circuit exhibits only one loop consisting of, Vg, L2, D2, L1, D3 and output group C-R. Because the inductors are coupled, for a simple analysis a simplified schematic is drawn, in Fig. 4, where the coupled inductors are modeled by an ideal transformer, noted IT, and a magnetizing inductance, LM, that it is equal with L1. We denoted the transformer ratio by n.

In order to determine the dc capacitor voltage and the static conversion ratio, the volt-second balance principle [6] for inductor LM, using Fig. 4, is written:

$$D\times V_g+(1-D)\times(\frac{V_g-V_c}{n+1})=0 \quad (1)$$

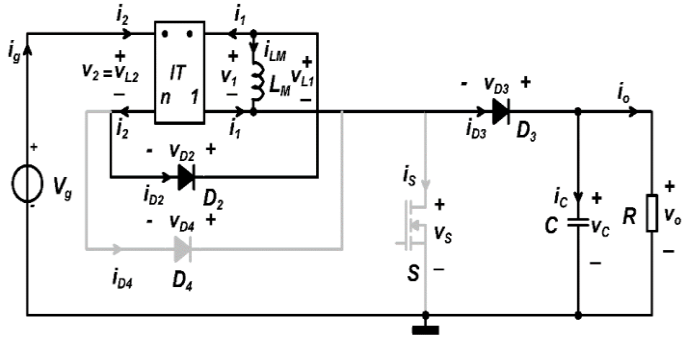

Figure 4: Model of proposed circuit

Definition:
D: Duty cycle (s)
V_g: Source (V)
V_c: Voltage acrross capacitor (V)
n: Transformer ratio
Reffer to (1):

$$V_c=V_o=\frac{1+n.D}{1-D}\times V_g \quad (2)$$

Hence the static conversion ratio of the converter is:

$$M=\frac{1+n.\mathrm{D}}{1-D} \quad (3)$$

According to (3) and Fig. 5, it can be observed that the output voltage is higher than the input voltage, the converter being of step-up type, with n>1 as a parameter. The conversion ratio of the new converter is higher than the one of a classical Boost converter, and even higher than that of the Hybrid Boost L converter from [8] (that is (1+D)/(1-D)), at the same duty cycle, if the transformer ratio is higher than unity. When the transformer ratio, n=1, the same static conversion ratio is equal to that in [8]. This proves the proposed converter a good choice for solar power systems where a high output voltages are needed.

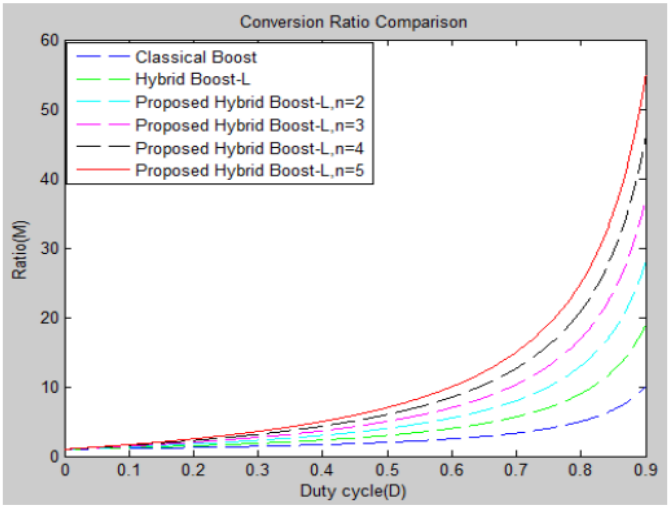

Figure 5: The static conversion ratio vs. duty cycle for the new converter and other Boost converters.

The dc inductor current is calculated as follows:

$$D\times(-\frac{V_c}{R})+(1-D)\times(\mathrm{I}_{LM}\times\frac{1}{n+1}-\frac{V_c}{R})=0 \quad (4)$$

$$\Leftrightarrow\frac{-D.V_c}{R}+\frac{I_{LM}}{n+1}-\frac{V_c}{R}-\frac{DI_{LM}}{n+1}+\frac{DV_c}{R}=0$$

$$\Leftrightarrow I_{LM}=\frac{n+1}{1-D}.\frac{V_c}{R} \quad (5)$$

Where: load R (Ω); dc inductor current I_{LM} (A)

From (2) and (5), the dc value of the magnetizing current can be rewritten as:

$$V_c=V_o=\frac{1+n.D}{1-D}\times V_g \quad (6)$$

The evaluation and worst case analysis requires the knowledge of components current and voltage stresses in the design process. The maximum voltage across switch S is calculated from the second topological state and is equal to V_C. With V_C given by (2), the transistor voltage stress is:

Nguyen Chi Hung and Ngo Dinh Thanh, "Design A Couple Inductor DC-DC Converter to Increase Conversion Ratio and Efficiency Using For Solar Energy System," *International Research Journal of Advanced Engineering and Science*, Volume 5, Issue 2, pp. 167-172, 2020.

International Research Journal of Advanced Engineering and Science
ISSN (Online): 2455-9024

$$V_S = \frac{1+n.D}{1-D} V_g \quad (7)$$

The current stress through the active switch S is I_{LM}, and from (6), the dc transistor current is:

$$I_S = D.I_{LM} = \frac{(n+1).(n.D+1).D}{(1-D)^2} \frac{V_g}{R} \quad (8)$$

The voltage stress across diode D_1 is $V_{LM}+V_C-V_g$, and by replacing V_{LM} from the second topological state, and V_C from (2), the diode D_1 voltage stress results in:

$$V_{D1} = \frac{n.D}{1-D} V_g \quad (9)$$

When on, current throught D_1 is equal to I_{LM} and from (6), it can be calculated as follows:

$$I_{D1} = \frac{(n+1).(n.D+1).D}{(1-D)^2} X \frac{V_g}{R} \quad (10)$$

The voltage stress across diode D_2 is equal to $V_2-V_g+V_1$, and by replacing with their equivalent from the first topological state, is obtained that:

$V_{D2} = n.V_g \quad (11)$

The voltage stress across diode D_3 is V_C, and by replacing with (2), it is obtained that:

$$V_{D3} = \frac{1+n.D}{1-D} \times V_g \quad (12)$$

The current through diode D_2 can be found from the second topological state, and is equal to i_2, that is also equal with i_1+i_{LM}. Also, diode D_3 current is equal with i_1+i_{LM}, and can be found from the second topological state, so the dc currents through D_2 and D_3 are:

$$I_{D2,3} = \frac{(n.D+1)}{1-D} \times \frac{V_g}{R} \quad (13)$$

From (7) and (12), it can be found that the voltage stress of both switch S_1 and diode D_3 are equal, and also the current stress of S and D_1, as (8),(10).

The magnetizing current peak to peak ripple can be given as:

$$\Delta i_{LM} = \frac{V_g.D}{L_M.f_s} \quad (14)$$

From (14) and (6), results the CCM condition for diode D_1:

$$\frac{2L_M.f_s}{R} \geq \frac{(1-D)^2.D}{(n+1).(n.D+1)} \quad (15)$$

The peak-to-peak capacitor voltage ripple can be found similar to the classical boost resulting in:

$$\Delta V_c = \Delta V_0 = \frac{V_C.\mathrm{D}}{R.C.\mathrm{f}_s} = \frac{V_g}{R.C.f_s} \times \frac{D.(1+n.D)}{(1-D)} \quad (16)$$

The equation (16) is used for selection the output capacitor. In realistic electric circuit, a ripple output still exists because of the nonzero equivalent series resistance (ESR) of the real capacitors.

In order to have a fair comparison, different step-up converters are supplied by the same input voltage V_g and delivering the same output voltage Vo, to the same load R are considered. The results are summarized in Table I.

Table I: Comparison between main parameters of different step-up converters.

Parameter	Type of Boost Converter			
	Classic	Hybrid Up1	Hybrid Up3	Proposed
Switches	1	1	1	1
Diodes	1	2	4	3
Total no. of components	4	8	8	7
System Order	2	3	3	3
Conversion ratio - M	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1+D}{1-D}$	$\frac{1+n.D}{1-D}$
Switch voltage stress	$M.V_g$	V_g	$M.V_g$	$M.V_g$
Switch current stress	$M.\frac{V_g}{R}$	$M.\frac{V_g}{R}$	$M.\frac{V_g}{R}$	$M(M-1)\frac{V_g}{R}$
Diode voltage stress	$M.\frac{V_g}{R}$	$\frac{(1-M).V_g}{2}$	$M.\frac{V_g}{R}$	$M.\frac{V_g}{R}$
Diode current stress	$M.\frac{V_g}{R}$	$M.\frac{V_g}{R}$	$M.\frac{V_g}{R}$	$M.\frac{V_g}{R}$
Input current	Smooth	Smooth	Smooth	Smooth

The statistics table above can see that: Although the DC-DC Boost conversions conducting the above study, although it is more complicated in terms of components and circuit structure, it provides an optimal efficiency when applying use. It can be clearly seen in the table above that the voltage conversion factor M has a significant increase compared to the rest of the topologies.

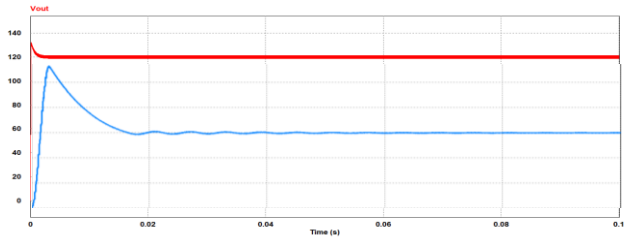

Figure 6: Waveform of Coupled Inductor Boost circuit output voltage (red) and Classic Boost circuit (green)

2.2. Design example for the proposed converter

It is desired to design the proposed boost converter according to the following specifications:

Input voltage: Vg = 30 V
Output voltage: Vo = 120 V
Output power: Po = 50 W
Switching frequency: fs = 50 kHz
Transformer ratio: n = 2

Because the input and output voltages are known, the static conversion ratio will result, M = Vo/Vg = 4.

Then using (3), the necessary duty cycle will be given by:

$$D = \frac{M-1}{M+n} = 0.5 \quad (17)$$

As R = V_o^2/Po, a value for the resistor of 288 Ω will be used. Imposing the inductor current ripples given by (14) the calculated inductor value is from (15), and we choose L_M=122.10 µH.

The value of LM will be equal with the value of L1, so $L_M=L_1$= 122.10 µH, and $L_2 = n_2 \cdot L_M$ = 488.40 µH.

Nguyen Chi Hung and Ngo Dinh Thanh, "Design A Couple Inductor DC-DC Converter to Increase Conversion Ratio and Efficiency Using For Solar Energy System," *International Research Journal of Advanced Engineering and Science*, Volume 5, Issue 2, pp. 167-172, 2020.

International Research Journal of Advanced Engineering and Science
ISSN (Online): 2455-9024

The output capacitor is calculated based on (16), with the voltage ripple to be 1% of output dc value. It result C_{min}=3.472 µF.

A value of 4.7 µF is chosen. The transistor voltage stress will be Vs = 120V, according to (7), from (8) its average current I_S = 1.25A. The diodes must be chosen to sustain a reverse voltage of V_D = 120 V, calculated with (12), and a dc current I_{D1} = 1.25A, given by (10).

III. Simulation Results

In order to evaluate the theoretical considerations, a simulation in Orcad software was performed. The values of the parts as below:

Vg = 30V, L1 = 122.10µH, L2 = 488.40µH, C= 4.7µF, R = 288 Ω.

All devices, including the diodes and the transistor, were chosen ideal. The gate of the transistor was driven by a PWM signal with the parameters:

fs = 50 kHz, D = 0.5

The dc output voltage Vo resulted from the simulation was 120 V in Fig.6, exactly as predicted by (3). In Fig. 7 the PWM signal for the gate of the transistor is shown. This PWM signal, may be measured by an oscilloscope. In Fig. 8, it can be seen the input current.

In Fig. 9, and Fig.10, the inductive voltage and current v_{L1} and i_{L1} are presented respectively. Because of the couple inductor, only half of the triangular shape of the magnetizing current will be seen, on the first inductor, and the other half triangular shape on the second inductor, Fig. 12. In Fig. 13, it can be seen the i_{LM} current, that is the triangular shape. The shape of the current together with the rectangular inductor voltage with two levels, indicate that the converter operates correctly in CCM.

The voltages across the second coil v_{L2} and the current i_{L2} are revealed in Fig. 11, and Fig.12 respectively, and again their shapes confirm CCM operation.

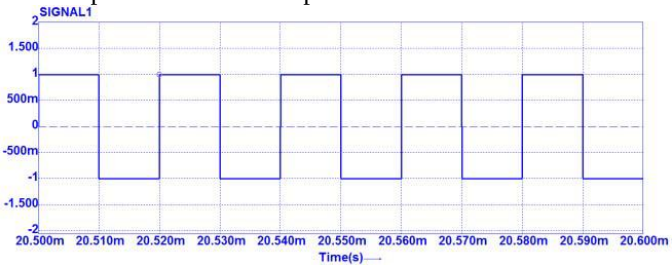

Figure 7: PWM signal applied to the gate of the transistor

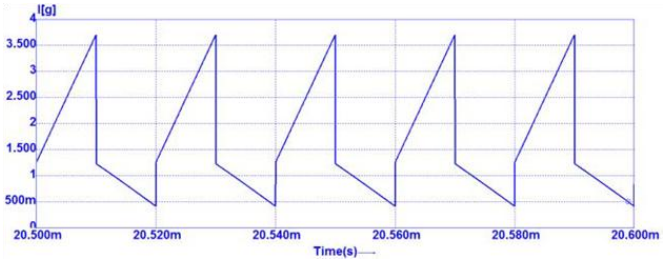

Figure 8: Input current

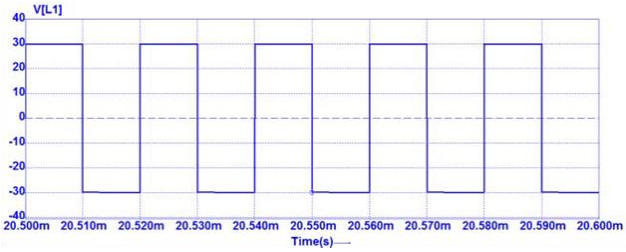

Figure 9: Voltage across the coil L_1

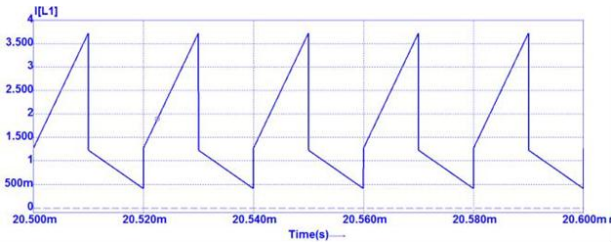

Figure 10: Current through inductor L_1

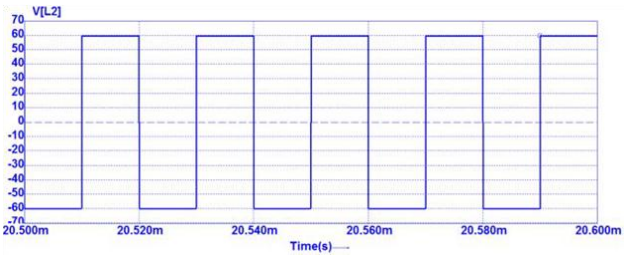

Figure 11: Voltage across the coil L_2

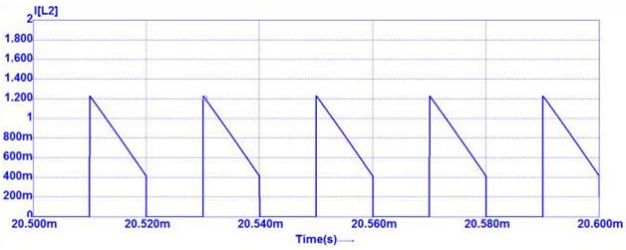

Figure 12: Current through inductor L_2

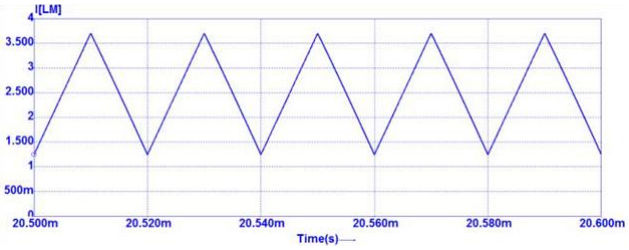

Figure 13: Current through the magnetizing inductor L_M

The theoretical calculate operation is validated by the Orcad simulations from above, and they demonstrate the correctness of the theoretical analyses.

IV. Experimental Results

A practical prototype similar to the simulated converter was built in order to study the real behavior of the converter and compare it to the theory. The components slightly differ from the designed values obtained in the previous paragraph and expect some slightly small differences because of parasitic

Nguyen Chi Hung and Ngo Dinh Thanh, "Design A Couple Inductor DC-DC Converter to Increase Conversion Ratio and Efficiency Using For Solar Energy System," *International Research Journal of Advanced Engineering and Science*, Volume 5, Issue 2, pp. 167-172, 2020.

International Research Journal of Advanced Engineering and Science
ISSN (Online): 2455-9024

elements in real devices (losses, imperfections and tolerances of electronic devices, etc.). The semiconductors are:

S = NXP MOSFET BUK455-200A, $D_{1,2,3}$ = Soft recovery ultrafast plastic rectifier UF5402, L_1 = 122.10µH, L_2 = 523.60 µH.

In Fig. 14 an oscilloscope capture is reproduced. As a reference, the first signal (in blue and labeled "Vds") is the voltage measured across the transistor. This signal will be displayed in all waveforms as a reference. It is a PWM signal with the same parameters as in the simulation. The second waveform is the output voltage (drawn with light blue and having the label "Vo"), and some spikes are present due to switching perturbations. The measured dc output voltage value is a little bit lower compared to theoretical calculation. The third signal depicted is the voltage across inductor L_1 (in red and labeled "v_{L1}"), exhibiting typical positive and negative levels. The last waveform is inductor L_1 current (shown in green, labeled "i_{L1}"). In Fig. 15, the first waveform is the voltage across the transistor that serves as a reference. The third one (with red and labeled "v_{L2}") is the voltage measured on the coil L_2. The last waveform is the current though inductor L_2 (drawn with green and having the label "i_{L2}"). It may be observed that the acquired waveforms are similar with the ones from simulation.

By varying the duty cycle D of the transistor and by measuring the output voltage Vo, the experimental static conversion ratio was measured. The comparison between the theoretical curve, losses theoretical curve and experimental results is depicted in Fig. 16. Only conduction losses are included in the losses theoretical model, more exactly the parasitic resistance that occurs in the circuits elements, and the forward voltage drops on the diodes.

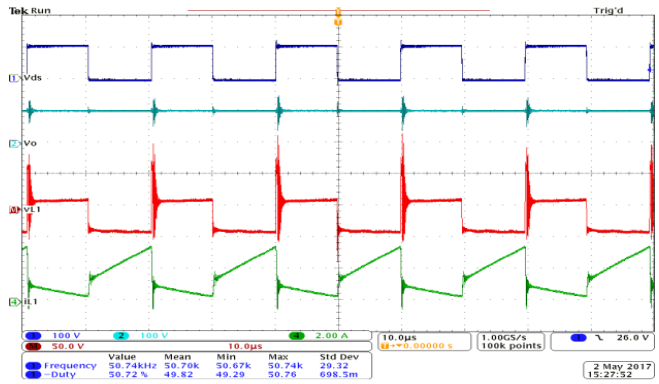

Figure 14: Oscilloscope waveforms: voltage across the transistor, drain to source (dark blue – V_{ds}); output voltage (light blue-Vo); voltage across L_1 (red- v_{L1}); current through L_1 (green- i_{L1});

The efficiency curve against the duty cycle is represented in Fig. 17.

The experimental curve closely follows the losses curve, and the fact it is below the theoretical losses characteristic is due mainly fault that the losses theoretical curve was calculated without assuming dc magnetizing inductor current. As can be seen, in Fig. 14, the inductor current exhibits also significant ripple that leads to additional losses. This also slightly decreases the efficiency compared to the theoretical losses curve.

It can be seen that excellent efficiencies, can be obtained. All these results confirm the feasibility and suitability of the proposed topology.

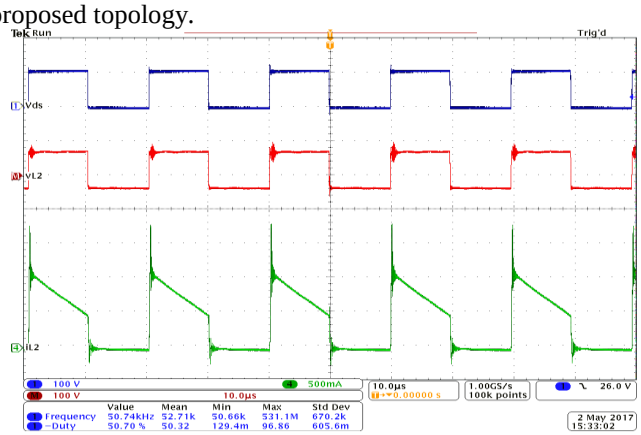

Figure 15: Oscilloscope waveforms: voltage across the transistor, drain to source (dark blue – V_{ds}); voltage across L_2 (red- v_{L2}); current through L2 (green- i_{L2});

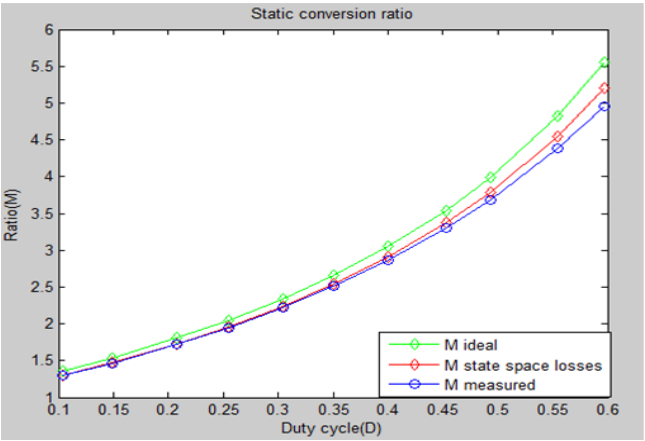

Figure 16: The experimental conversion ratio against duty cycle in comparison with the ideal, respectively with losses calculated.

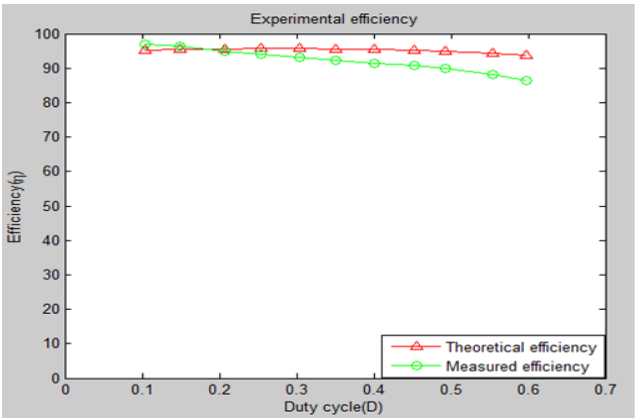

Figure 17: The experimental efficiency against the duty cycle

V. Conclusion

The proposed coupled inductor DC-DC converter is a method in order to boot the output voltage higher than the input one as it still operates at narrow duty cycles, while

Nguyen Chi Hung and Ngo Dinh Thanh, "Design A Couple Inductor DC-DC Converter to Increase Conversion Ratio and Efficiency Using For Solar Energy System," *International Research Journal of Advanced Engineering and Science*, Volume 5, Issue 2, pp. 167-172, 2020.

maintaining high efficiency. The topology uses only one transistor, three diodes, and one coupled inductors. The static conversion ratio is (1+nD) time higher than a classical Boost at the same duty cycle D. Steady state analyses, and a comparison with other converters are performed. To validate and confirm our theoretical assumptions, it is simulated by Orcad simulation program. Therefore, how it is obvious from the theoretical calculation, compared to the simulation waveforms can be seen a very good accordance. Experimental results confirm the simulation and theory. The proposed converter could be a simple and cheap solution in solar power systems where an output voltage much higher than input voltage is needed.

REFERENCES

[1] 19th International Symposium POWER ELECTRICS Ee2017, October 19-21, 2017, Novi Sad, Serbia

[2] (The Oxford Series in Electrical and Computer Engineering) Adel S. Sedra_ Kenneth C. Smith-Microelectronic Circuits-Oxford University Press (2014)

[3] Research DC/DC boost topology with neutral point with DC source_Quach Thanh Hai, Truong Viet Anh, Le Hoang Phi_ HCMC University of Technology and Education

[4] Chapter 4: DC-DC Converters_ Tran Quoc Hoan, PhD

[5] S. Ćuk, "A new zero-ripple switching DC-to-DC converter and integrated magnetics," IEEE Trans. on Magn., vol. 19, no. 2, pp. 57-75, March 1983.

[6] R. W. Erickson and D. Maksimovic, Fundamentals of Power Electronics, 2nd Ed., Chapman and Hall, 2001.

[7] D. Maksimovic and S. Ćuk, "Switching Converters with Wide DC Conversion Range," IEEE Trans. on Power Electron., vol. 6, no. 1, pp. 151-157, January 1991.

[8] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Switched capacitor/switched inductor structures for getting transformerless hybrid dc-dc PWM converters," IEEE Trans. on Circuits & Systems-I, vol. 55, no. 2, pp. 687-96, March 2008.