

Electronic Package with ESD/EOS Protection Component

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I. BACKGROUND OF THE STUDY

- As the die technology becomes smaller, thinner, and faster, silicon die circuit metallization also becomes smaller, thus the electronic devices like that of the quad flat package (QFP) and quad flat no-leads (QFN) semiconductor leadframe package shown in Fig. 1 become more sensitive and susceptible to electrical overstress (EOS) and/or electrostatic discharge (ESD) damages

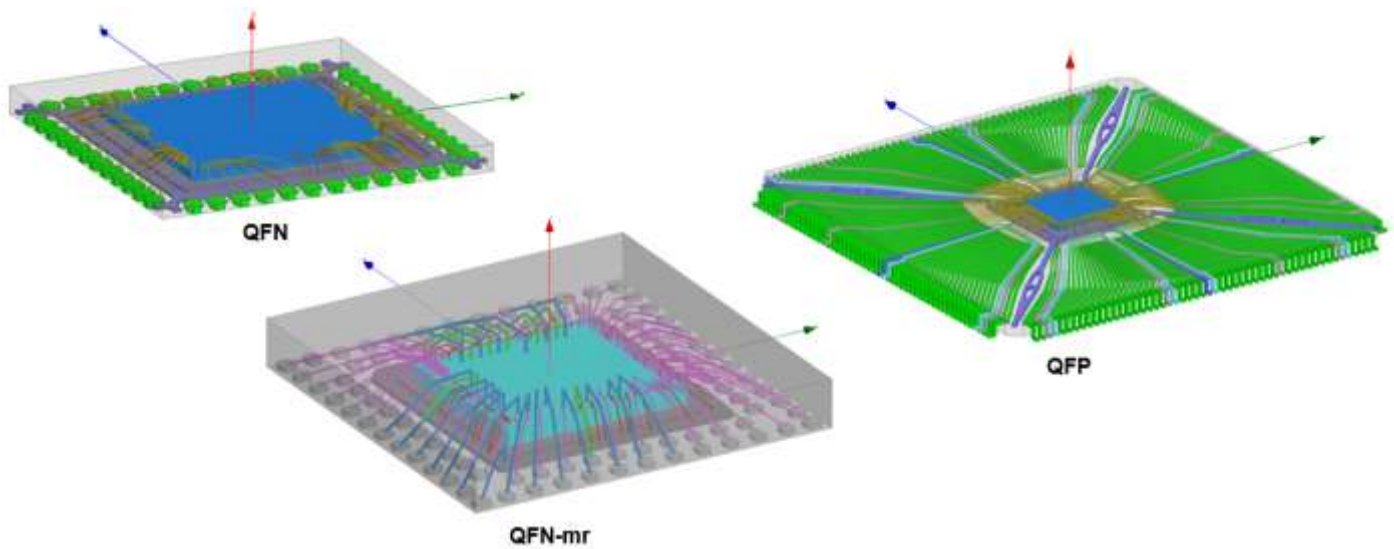


Fig. 1. Electronic packages of leadframe configurations.

- With time-to-market customer needs becoming more demanding, there is a necessity to adapt to the latest trends, prevent package-related issues, and address issues at the soonest as possible

II. PROBLEM IDENTIFICATION

- Some electronic packages haven't integrated yet the EOS/ESD protection circuitry at the die or transistor design level, making these packages susceptible to EOS/ESD-related anomalies or damages
- An example of such defect manifestation is shown in Fig. 2, with the package eventually destroyed

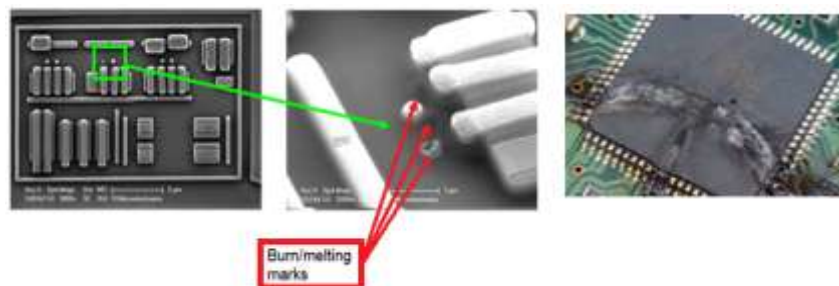


Fig. 2. Examples of EOS/ESD defect manifestation.

III. ELECTRONIC PACKAGE DESIGN SOLUTION

- The electronic packages in semiconductor leadframe configuration are embedded with EOS/ESD protection component with the EOS/ESD diode on the leads and/or the silicon die, as illustrated in Fig. 3
- The EOS/ESD diode could be mounted or attached using conductive/sintered glue, solder bump, or any conductive adhesive material between the lead or signal pin and the diepad or ground, and could also be mounted between any two signal pins or leads
- The protection components could also be embedded or attached on the silicon die or the active die through the bond pads using conductive/sintered glue, solder bump, or any conductive adhesive material

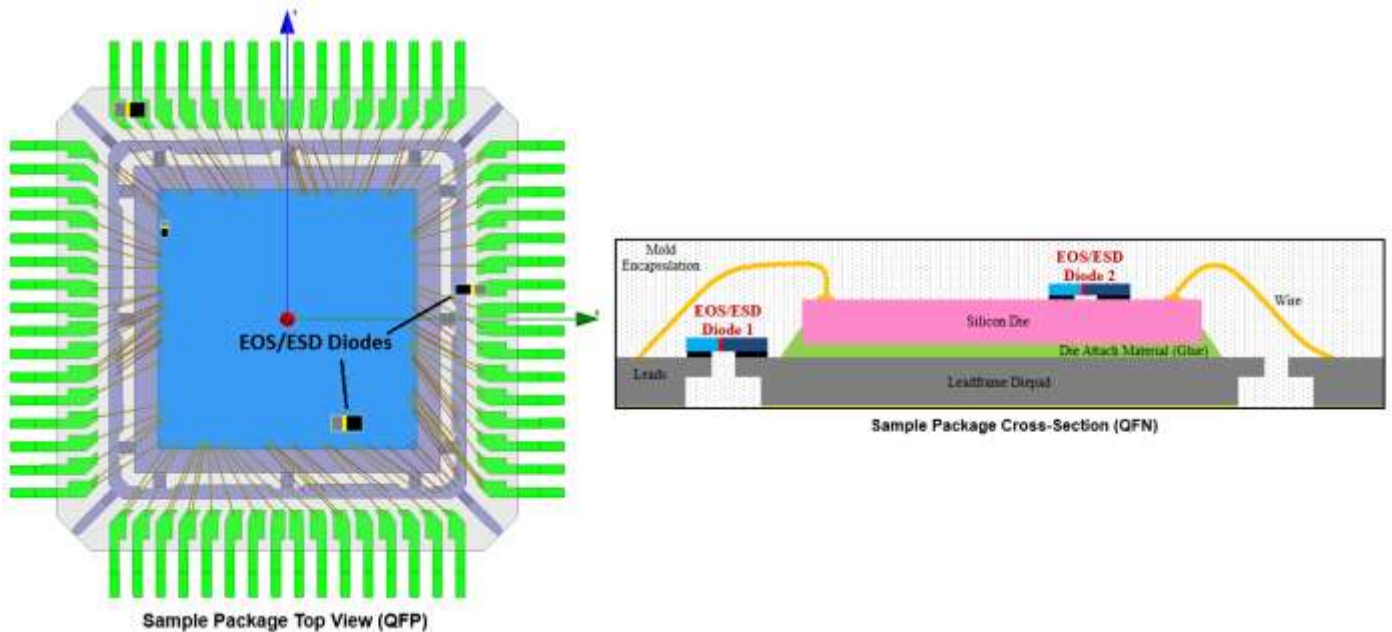


Fig. 3. Electronic packages of leadframe configurations, with embedded ESD protection components.

- By incorporating EOS/ESD protection components inside the electronic package, EOS/ESD-sensitive packages without internal EOS/ESD die circuitry could now be protected against eventual EOS/ESD-related defects or anomalies