

Improved and Cost-Effective Coating Film for Wafer Level Electronic Package

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Abstract — In semiconductor assembly manufacturing wherein the competition is tough among all the semiconductor industries, one main factor to consider is the cost of a material. This paper discussed how the product was managed to be competitive in terms of manufacturing cost. The components were critically analyzed to eventually achieve the project goal and identify ways in reducing package cost that impacts the company's profit.

Keywords— Semiconductor; wafer level; assembly; wafer coating film; manufacturing.

I. INTRODUCTION

Wafer level electronic package is one of the top rising products in the market. And during assembly manufacturing, package cost is greatly influenced by the choice of the materials used. Be it direct or indirect materials, one must have a very competitive price to strive in the market. This is one of the biggest challenges for any semiconductor company in order to maintain its competitive market position and value. There are various components for the device that needs to be carefully analyzed and evaluated to obtain cost-efficient device or products, that eventually will drive customers to enter business with the manufacturing plant.

Yearly there is price erosion, thus, semiconductor manufacturing companies drive cost reduction measures to maintain good business. Analyzing the current manufacturing cost of wafer level electronic package (hereinafter referred to as Device C) is one of the main activities performed to maintain a healthy business relationship with customers, maintaining high quality at the same time. Device C has one of the highest local manufacturing cost, and this directly impacts the overall product cost of the device. To support the drive for cost reduction, main contributors of the high cost were identified and one of which is the wafer coating film material. This coating material for silicon die needs to be critically analyzed and improved. Shown in Fig. 1 is the typical assembly process flow of the product.

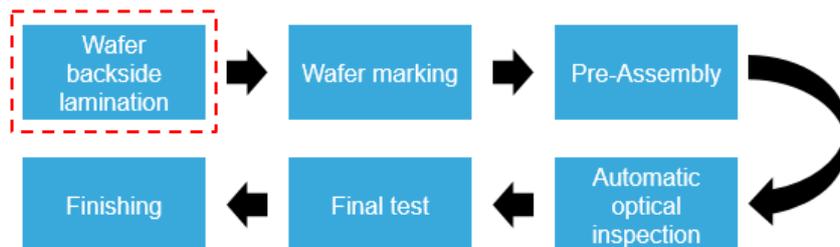


Fig. 1. Typical manufacturing process flow of the electronic package.

II. PROCESS SOLUTION AND IMPROVEMENT, AND DISCUSSION OF RESULTS

Wafer coating film is a direct material of Device C, which is attached on the wafer backside through lamination process, as depicted in Fig. 2. The main purpose of the study presented on this paper is to have significant improvement on the wafer backside lamination process using a cost-effective wafer coating film material, in order to meet the assembly manufacturing low cost target or requirement. This new wafer coating film has an advantage during the wafer sawing process thus preventing chipping compare to the original material with some issues encounter.



Fig. 2. Coating film lamination to wafer backside.

This new improved and cost-effective wafer coating film blocks off light, minimizing its effect on the circuit surface. This also results to no major issue or negative effect during its product reliability. Highlighted in Fig. 3 is the comparison of the previous wafer coating film material and the improved one in terms of cost.

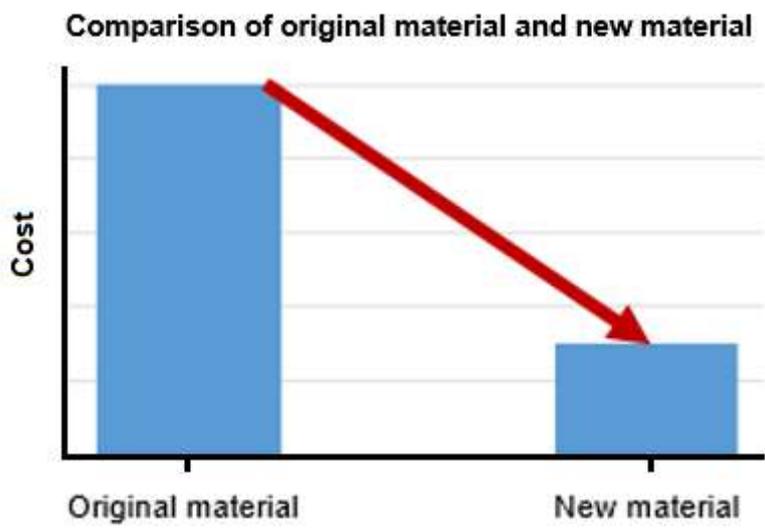


Fig. 3. Comparison of wafer coating film materials (actual values intentionally not shown).

The comparison shows the new wafer coating film material being cost-effective, with improvement in cost of almost 60% lower compared to the original material. This project achieved the goal to maintain cost competitiveness, and the risks brought by the material change were carefully assessed and reviewed to ensure it will not affect the end-product. Ultimately, the project successfully met the product requirement of the customer using the improved and cost-effective material.