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Realization of a Miniaturized BGA Package

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I. BACKGROUND

A ball grid array or BGA semiconductor device is a type of surface mount packaging used in integrated circuit (IC) with the silicon die wired/connected to the bond fingers and metallic inter-layers of the substrate. The inter-layer metallic routing distributes the connection to the defined input/output (I/O) location, as shown in Fig. 1.

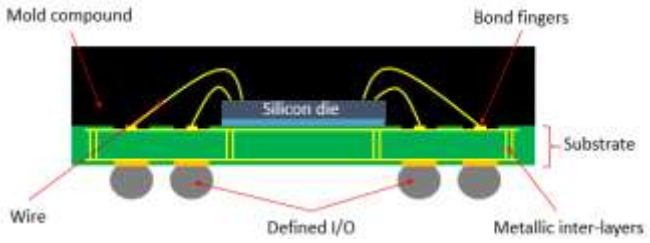

Fig. 1. BGA package model cross-section.

The primary advantage of BGA device is it can accommodate more interconnection pins that can be available on the whole backside footprint of the device. Note that a typical quad flat no-lead (QFN) device has its interconnection pins available at the perimeter only.

II. PROBLEM IDENTIFICATION

BGA design and architecture is known to cater higher count of I/O interconnect through the use of substrate technology. An example of BGA device is given in Fig. 2.

Fig. 2. An example of a BGA semiconductor package.

However, the problem for this package configuration is that it requires additional spaces and clearances inside the substrate construction which creates a bigger package dimension in comparison to other surface mount technology. The transition of BGA product to a downsized version is a major detractor of package miniaturization of semiconductor packages.

III. PROCESS AND PACKAGE DESIGN SOLUTION AND IMPROVEMENT

A miniaturized version of a BGA can be realized through improvement in the silicon die design architecture wherein the backside portion is maximized and will be fabricated with active circuit, as showcased in Fig. 3.

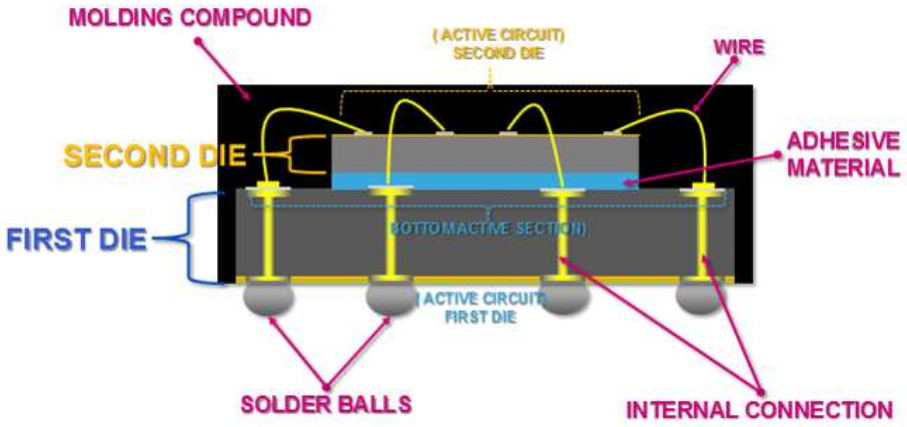

Fig. 3. Silicon die architecture with bottom active section.

Furthermore, some of the interconnection could be incorporated in the bottom active section design which will lessen the metallic interlayers in the substrate.

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