

Realization of a QFN with Multiple I/O Interconnection Robustness

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I. OVERVIEW

- Nowadays, the current technology for Quad flat no-grid multi row (QFN-mr) packages are restricted only to dual arrays of I/O (input/output) due to the assembly and process limitations for triple arrays of I/O design for QFN. During implementation of triple or more arrays of I/O, different assembly challenges especially from wirebond and molding process are highlighted.
- One of the inputs from wirebond process related to the design of triple or more arrays of I/O is the occurrence of long wire connection between the silicon die and the 3rd array of I/O.
- A long wiring connection/lay-out is susceptible to instabilities during molding process where wire shorting happens when the mold fillers bumps to the wire during encapsulation process creating displacement in the wiring structure.

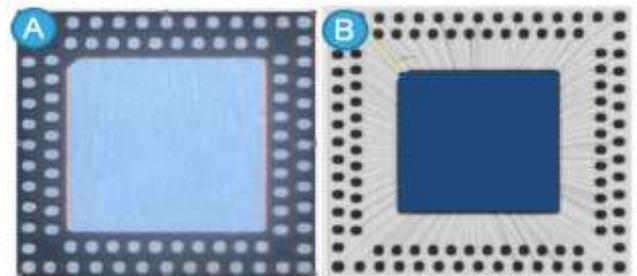


Fig. 1. (A) Sample photo of a device with dual arrays of I/O, (B) Wire shorting rejection on long wire connection.

- In addition, another negative limitations is the clearance of each individual I/O becomes smaller when the number of I/O is increase leading to complex and “wire crossing” scenario on the actual design lay-out.

II. PACKAGE DESIGN SOLUTION

- A QFN-mr with routed interconnection design is recommended for the design and construction of QFN multi-row packages that require triple or more arrays of I/O connection.

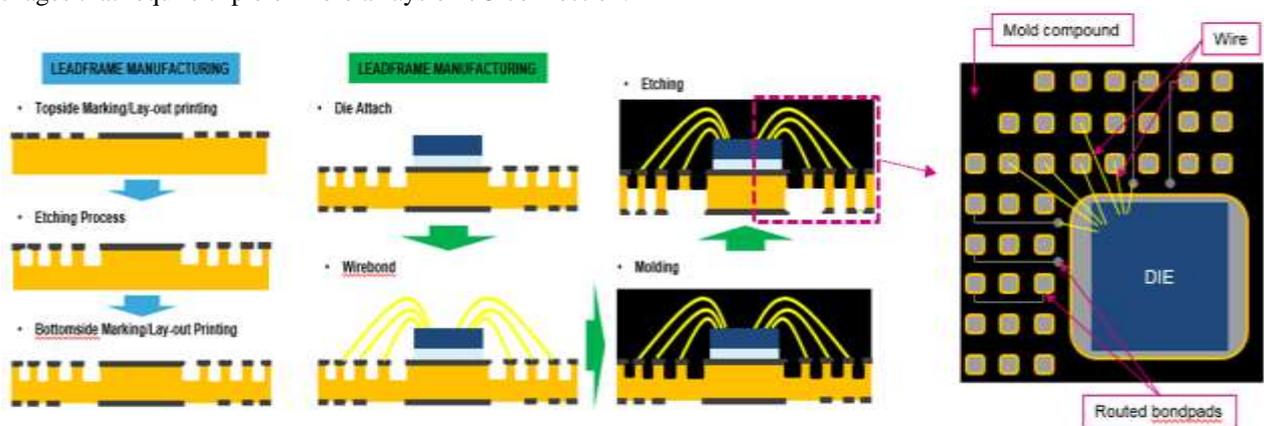


Fig. 2. Illustration of a device with routed I/O interconnection.

- The routing of the I/O interconnects can be done using two kinds of connection lay-out, (1) through connecting the 3rd arrays of I/O on the first or second blank I/O, (2) the 3rd array could have separate connection route which the wiring can be connected.