

Understanding the Impact of Underfill Fillet: A Key to Die Crack Elimination in FCBGA Packages

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I. OVERVIEW

- Flip chip ball grid array (FCBGA) package is a laminate substrate-based semiconductor package with silicon die having solder bump for providing electrical connection between the active die side to the substrate as shown in Fig. 1. This eliminates the use of wire bonding to connect the die bond pad to the substrate pad.

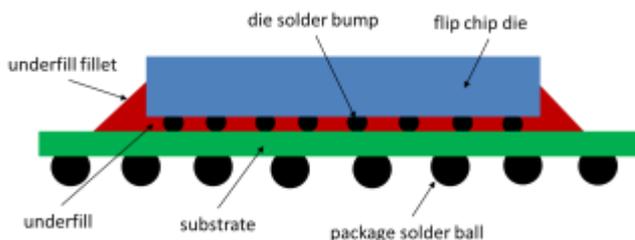


Fig. 1. FCBGA package.

- For FCBGA package, underfill material is generally used to absorb stress when the package is subjected to thermal cycling and other mechanical loading. It supports the die solder bump so that the electrical connection from the die to the substrate would remain intact.

II. PROBLEM IDENTIFICATION

- Die crack was encountered in a bare die FCBGA package after thermal cycling. Fig. 2 shows the image of the actual die crack.

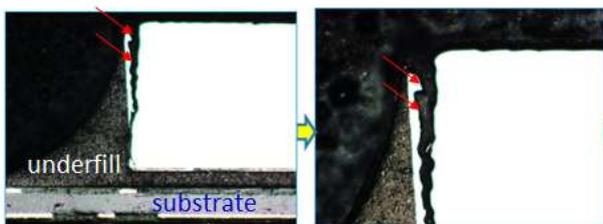


Fig. 2. Die crack at the side of the silicon die.

- The initiation of die crack was at the intersection of the underfill fillet edge and the die side surface.
- There was no crack in the die solder bump connection to the substrate.

III. STRESS ANALYSIS

- Finite element analysis (FEA) was conducted considering temperature loading since the failure happened after thermal cycling.
- Die stress at the side surface of the die was analyzed to understand the impact of underfill fillet on the die crack issue.

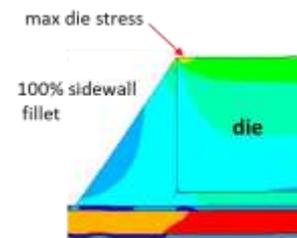


Fig. 3. Stress analysis result showing location of maximum die stress.

- As shown in Fig. 3, maximum die stress (tensile stress) is also located at the area where the actual die crack initiated. This means that as the underfill shrinks during the low temperature part of the thermal cycling, high stress is induced in the die causing die crack.

IV. PROCESS AND PACKAGE DESIGN SOLUTION AND IMPROVEMENT

- Reducing the underfill fillet during underfilling process would help eliminate die crack since die stress becomes lower as shown in Fig. 4.
- A new underfill material with lower coefficient of thermal expansion (CTE) and modulus could also be used as well as reducing the thickness of the substrate.

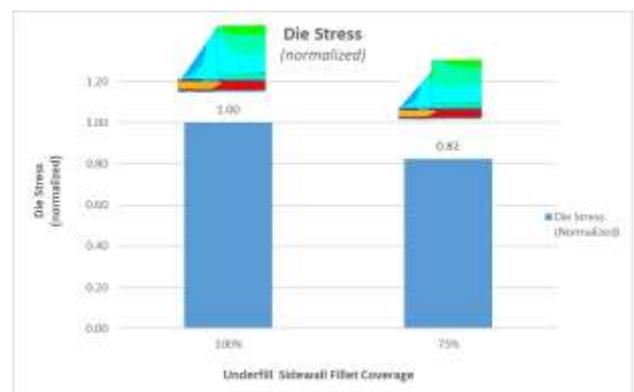


Fig. 4. Die stress vs underfill sidewall coverage (%).