

Transforming Mold Process Capability towards a Cost Effective Solution

Ernesto Antilano Jr.

Central Engineering & Development, Backend Manufacturing and Technology
 STMicroelectronics, Inc., 9 Mountain Drive, LISP II, Calamba 4027 Laguna, Philippines

Abstract— Encapsulating a semiconductor device is achieved by using either Compression molding or Transfer molding. Compression molding is highly recommended in a map configuration, like in quad flat no leads (QFN) packages, with a very complex wirebonding profile characterized by long wire span and thinner wire diameter. However, on a configuration like chip on leads (COL) with very limited wires, profit margin is compromised due to the direct and indirect materials cost contribution. Herein, evaluation of transfer molding is explored for package feasibility, cost benefit and process capability. All potential risks and defined mitigation plans are carefully assessed to achieve product manufacturability on a thin mold profile.

Keywords— Compression molding, transfer molding, chip on leads, process, capability.

I. INTRODUCTION

Compression molding provides a lot of advantage in terms of process capability and yield performance, most especially when it comes to molding a complex device on a one-map configuration (Fig. 1). However, one of the biggest challenges when using the compression molding is the granular molding compound and the mold release film, which are very expensive adding significant increase to the device unit cost. In addition, the limited capacity of the compression molding tool i.e., single cavity molding makes the process prohibitive in cost reduction projects. Hence, evaluation of transfer molding was initiated to reduce the overall assembly cost of the products.

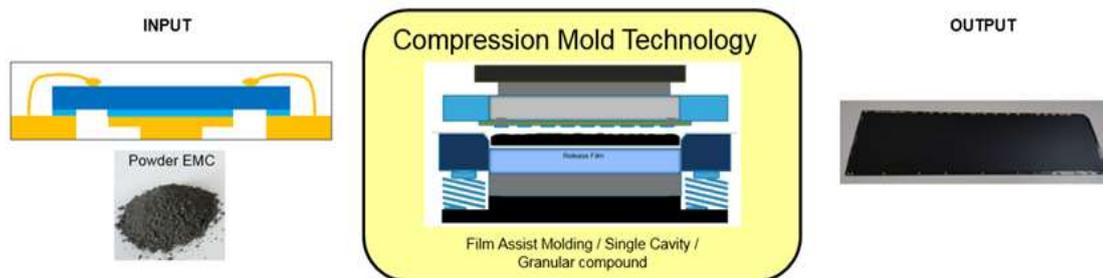


Fig. 1. Compression molding process using granular molding compound on a single cavity with film assist molding.

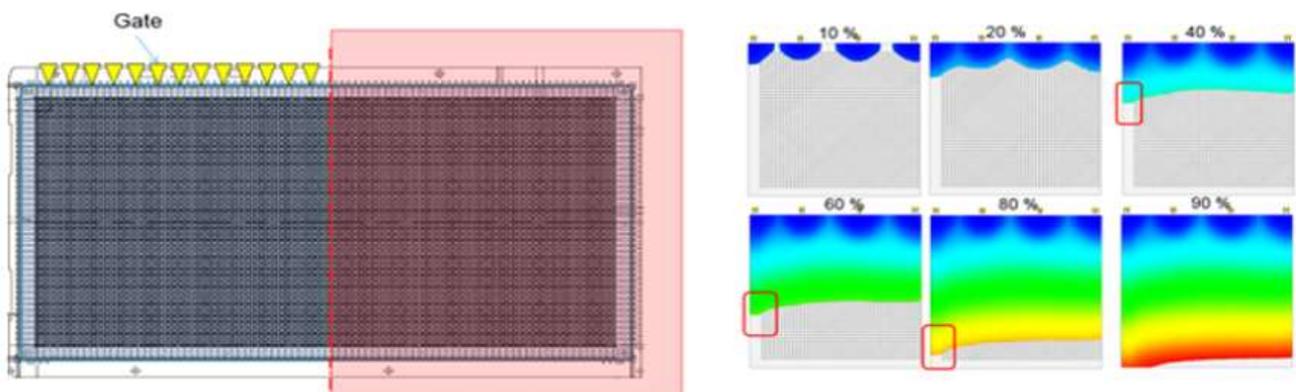




Fig. 2. Mold flow simulation with highlighted point at the critical area near the air vent side. Short shot reveals a balanced mold compound flow.



Fig. 3. Transfer molding process using pelletized molding compound on a dual cavity.

To reduce the risks and resources prior the actual evaluation, mold flow simulation was performed in collaboration with the mold tool supplier (Fig. 2). Results of the simulation were correlated with the short shot process performance. Moreover, the introduction of the transfer molding with dual cavity increased the mold process capacity, resulting in higher productivity.

II. DESIGN AND PROCESS SOLUTION

With the drive towards cost reduction, a feasibility study was conducted to ensure process capability on a QFN-COL package configuration. Assessment of the potential risks and mitigation plans were considered. Design review of materials and tooling, as well as mold flow simulation were requested to capture any process related failures before the actual evaluation. Short shot process was performed to understand the mold compound flow profile. Dummy shots were tested on

Transfer Molding for visual and dimensional check (Fig. 3). The final mold shot using populated wirebonded die on strips were subjected to wire sweep measurement and SCAT inspection for any mold defects induced at the mold process. Results indicate that transfer molding process with the given package configuration can be achieved with a thorough assessment of materials and processes.

III. CONCLUSION

With a comprehensive approach on identifying potential risk on process capability and product manufacturability, transfer molding process exhibits promising potential. Introduction of this new process capability on a map configuration will definitely increase the production capacity and improve the profit margin.

REFERENCES

- [1] Mian Zhi Ding; Boon Long Lau; Zhaohui Chen. Molding process development for Low- Cost MEMS-WLCSP with silicon pillars and Cu wires as vertical interconnections 2017, IEEE 19th Electronics Packaging Technology Conference (EPTC), 6-9 Dec. 2017
- [2] L.E. Felton; N. Hablutzel; W.A. Webster; K.P. Harney. Chip scale packaging of a MEMS Accelerometer 2004 Proceedings. 54th Electronic Components and Technology Conference IEEE Cat. No.04CH37546, 4-4 June 2004
- [3] D.W. Palmer; D.A. Benson; D.W. Peterson; J.N. Sweet. IC chip stress during plastic package Molding 1998 Proceedings. 48th Electronic Components and Technology Conference Cat. No. 98CH36206, 25-28 May 1998