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Overcoming Design Challenges on Ultra-Thin Substrate-based Packages

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Abstract— *Ultra-thin substrate-based package is one of the promising technologies that can offer a large variety of geometrical possibilities, specifically for the telecommunications industry. One eminent technology is a foldable mobile phone in which miniaturization of internal components provides a major challenge in the manufacturing and assembly processing. In order to achieve ultra-thin based packages, thinned silicon and low loop wirebonding profile must be applied to provide appropriate dimension in the packaging technology. In addition, to overcome these design challenges, copper carrier was explored. The assembly process includes a pre-mount copper carrier on ultra-thin substrate which offer stiffness during the handling process from die attach assembly, wirebonding and mold encapsulation. After molding process by compression, the copper carrier is stripped off to expose the ball land on a ball grid array package for the next assembly process.*

Keywords— *Ultra-thin substrate-based packages, copper carrier, compression molding.*

I. INTRODUCTION

In order to stay on top of the mobile phone competition, innovation and process capability must be exceptional, especially since end users are longing for a thinner, lightweight, compact and flexible device. Development of this ultra-thin substrate-based package offers excellent advantage in terms of room capacity for electronic module in a complex assembly. Using a standard substrate thickness (Fig. 1), assembly processing is not a concern. However, reduction of the substrate thickness without reinforcement can lead to manufacturability problems.

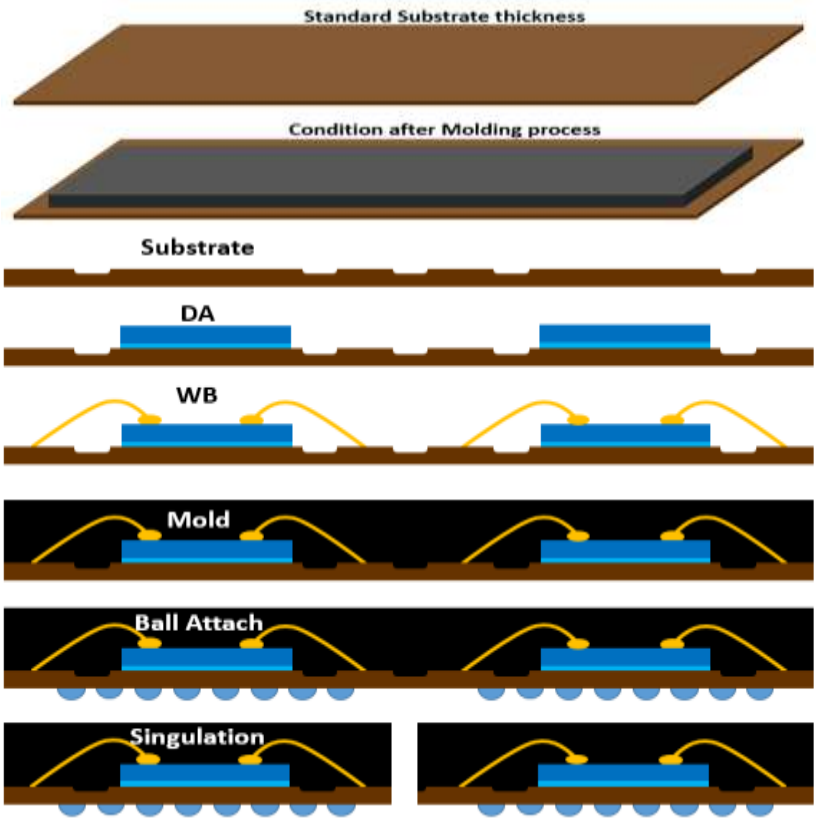

Fig. 1. Incoming substrate condition using standard thickness and the package assembly flow. DA – die attach; WB – wirebond.

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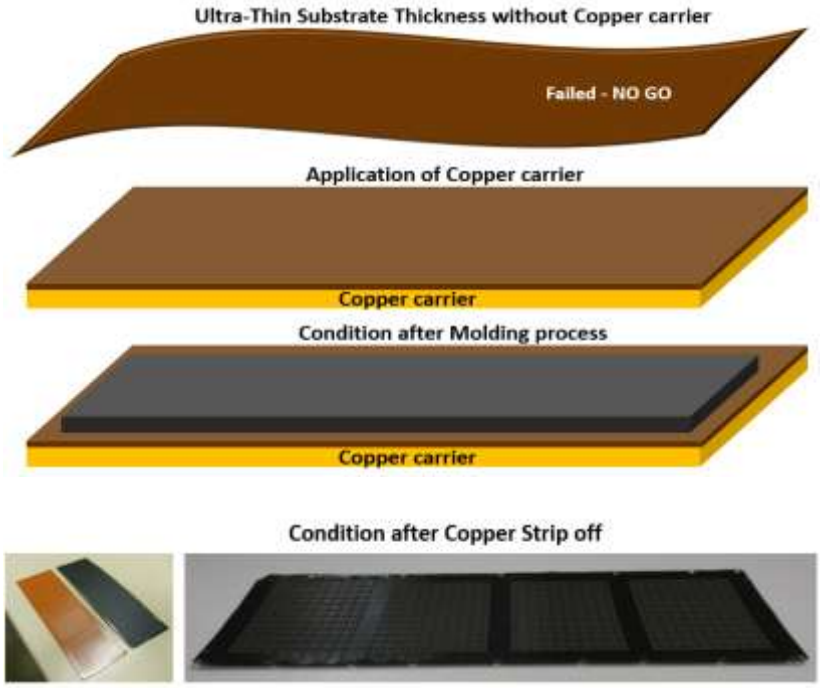

Fig. 2. Application of copper carrier on ultra-thin substrate which offers additional stiffness during the handling process.

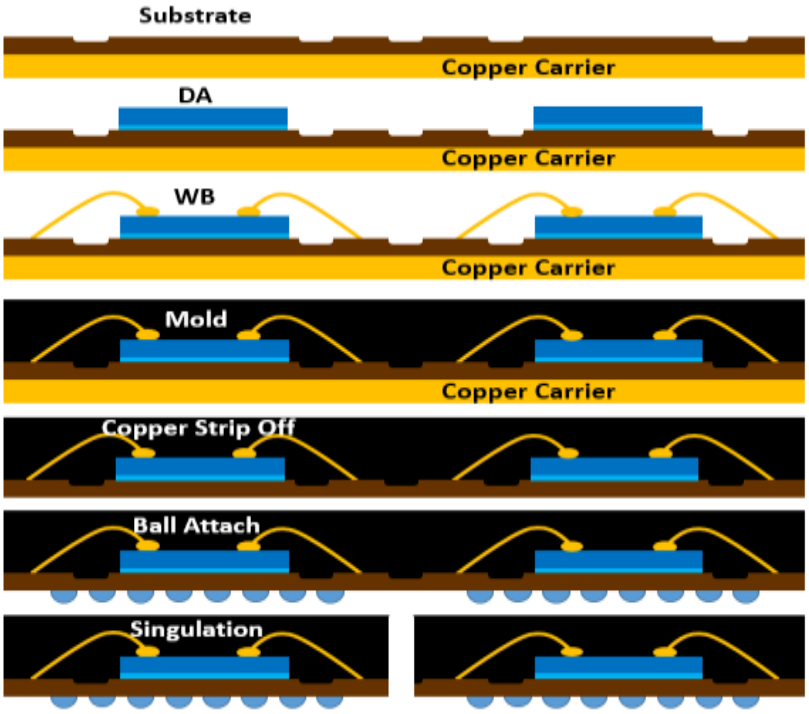

Fig. 3. Package assembly flow using a Copper carrier. DA – die attach; WB – wirebond.

In order to manage assembly processing for ultra-thin substrate-based packages, a low cost copper carrier was introduced (Fig. 2). Additionally, reduction in machine downtime on handling the ultra-thin substrate, risk mitigation and efficient resources management were implemented, resulting in higher productivity.

II. Design and Process Solution

Overcoming this design challenge on a manufacturing process, a pre-mounted copper carrier on ultra-thin substrate, which offers stiffness during handling process was introduced. The assembly flow starts from substrate carrier transfer into slotted magazine, die attach assembly, wirebonding and mold encapsulation (Fig. 3). This copper carrier on extremely thin

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substrate design is stripped off after mold compression process to expose the ball land on a ball grid array (BGA) package for the next process assembly.

One of the primary advantages is the low cost material, compatible to all process assembly and can be easily stripped off without any stress induced. Generally, it can be re-used through supplier partnership. Moreover, manufacturing process from die attach, wirebond, mold encapsulation to ball attach will be achieved via standard process.

III. Conclusion

Overcoming the design challenge by the use of copper carrier on extremely thin substrate-based package enables manufacturability of an extremely thin substrate-based process. Introduction of this innovation offers the possibility of a robust process, critical in the success of this next generation device.

References

[1] Yu Sun; Xiaofeng He; Zhongyao Yu; Lixi Wan Development of ultra-thin low warpage coreless substrate. 2013 IEEE 63rd Electronic Components and Technology Conference 28-31 May 2013

[2] W. Schwarzenbach; X. Cauchy; O. Bonnin; F. Boedt; E. Butaud; C. Moulin; S. Kerdiles; J.-F. Gilbert; N. Daval; C. Aulnette; C. Girard; M. Yoshimi; M. Yoshimi Ultra Thin silicon substrate for next generation technology nodes. 18-20 Oct. 2010 2010 International Symposium on Semiconductor Manufacturing (ISSM)

[3] B. Pahl; C. Kallmayer; R. Aschenbrenner; H. Reichl Ultrathin assemblies on flexible substrates 2005 7th Electronic Packaging Technology Conference 7-9 Dec. 2005.