

Process Punch Design Augmentation for Chip-Out PPM Trend Improvement

Antonio R. Sumagpang Jr., Frederick Ray I. Gomez

Central Engineering & Development NPI, Back-End Manufacturing & Technology, STMicroelectronics, Inc.
Calamba City, Laguna, Philippines 4027

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I. BACKGROUND OF THE STUDY

- Package chip-out is a process defect recorded during the singulation stage at the trim and form process in Fig. 1 of semiconductor assembly manufacturing

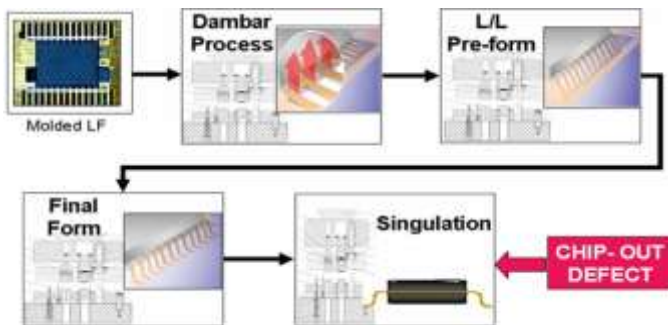


Fig. 1. Process mapping.

- Package chip-out is defined as a region of material missing from a body as shown in Fig. 2



Fig. 2. Package chip-out location at the upper left of the package.

- The singulation punch in trim and form process guides and holds the package units to singulate from the leadframe matrix, and requires a critical dimension in order to perform its required function
- Illustration in Fig. 3 shows how the unit is being singulated in case the singulation punch does not comply with the required dimension

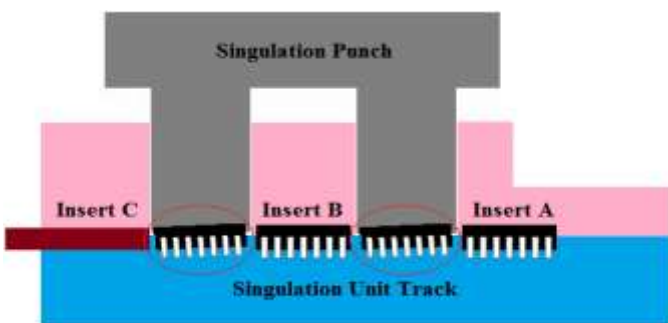


Fig. 3. Possible mis-alignment during package singulation.

II. PROCESS DESIGN SOLUTION

- Computer simulation and tool adjustment in Fig. 4 were done under worst condition, showing maximum shift of package to the left most of the singulation punch

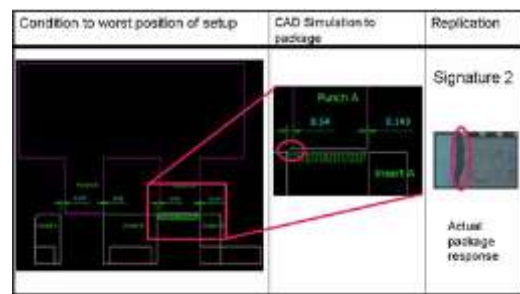


Fig. 4. Simulation and replication of package chip-out signature.

- The peripheral dimensions of the singulation punch design in Fig. 5 were augmented and improved based on the simulation and replication of the package signature chip-out

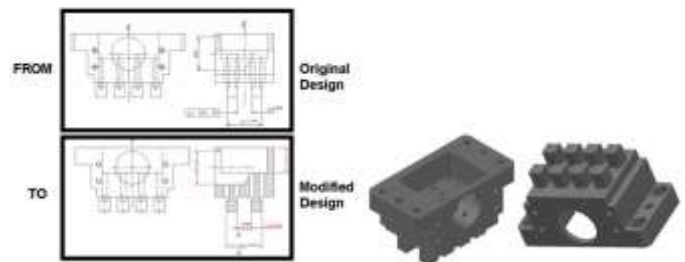


Fig. 5. Singulation punch design augmentation and 3D modeling.

- The simulation and replication made via design augmentation and improvement contributed to a significant improvement in end-of-line (EOL) parts per million (PPM) reduction of package chip-out in Fig. 6

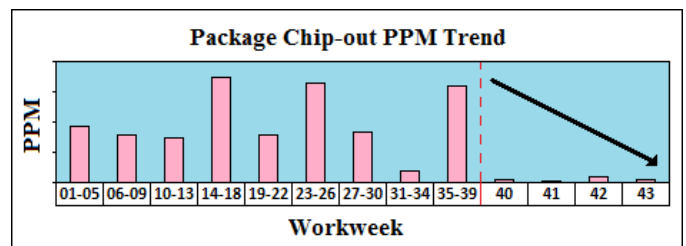


Fig. 6. Package chip-out PPM trend improvement (actual PPM not shown).