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Advance I/O Design for Multiple Wirebond Layout Configuration

Rennier S. Rodriguez, Frederick Ray I. Gomez
Central Engineering & Development NPI, Back-End Manufacturing & Technology, STMicroelectronics, Inc.
Calamba City, Laguna, Philippines 4027

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I. Overview

- Leadframe is the common indirect material used in semiconductor quad flat no-leads (QFN) assembly to interconnect the silicon die to board level
- The number of input/output (I/O) leads or signals depends on the end-product application
- Each I/O is wirebonded to the die using gold or copper wirebond material

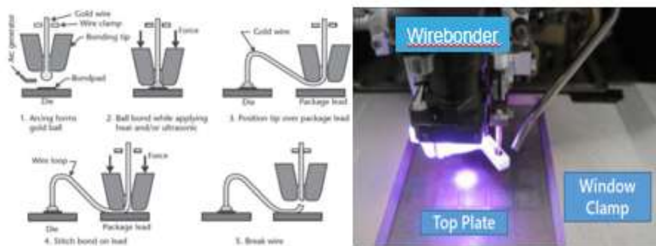

Fig. 1. Wirebonding process.

II. Problem Identification

- For multiple I/O leadframe configuration, the bonding of wire is restricted according to the position of the bondpads against the required location of the I/O inside the leadframe

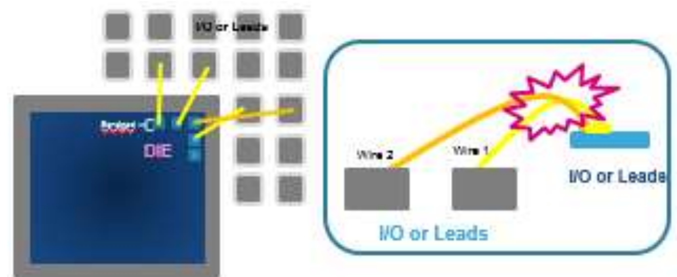

Fig. 2. Wire shorting reject on multiple I/O configuration.

- Wire crossing or wire overpassing a neighboring wire should be avoided during wirebond layout, due to probability of shorting connections
- Wire shorting could also occur during mold encapsulation process for wire connections with small or tight clearances

III. Package Design Solution

- An advanced I/O design of leads of the semiconductor QFN package with complex wirebond layout is presented in Fig. 3
- The improved leadframe design incorporates a connection bars between two I/O leads that is required to retain electrical inter-connection

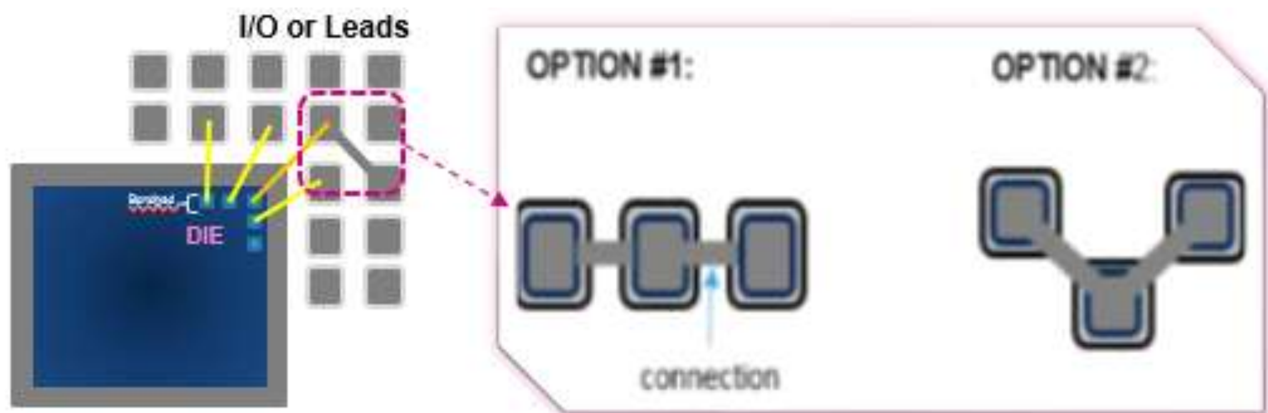

Fig. 3. Advanced lead design for multiple I/O interconnect.

- Wire shorting and related wirebond anomalies could be mitigated through incorporating the improved design of leads