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Semiconductor IC Package Leakage Current Improvement

Frederick Ray I. Gomez
New Product Introduction Department, Back-End Manufacturing & Technology, STMicroelectronics, Inc., Calamba City, Laguna, Philippines 4027

Abstract*—This technical paper presents the improvement in the leakage current performance of Semiconductor Integrated Circuit (IC) packages by eliminating the Electrostatic Discharge (ESD) events during assembly process and ensuring the proper machine grounding and ESD controls. It is of high importance to significantly reduce or ideally eliminate the leakage current failures of the device to ensure the product quality, especially as the market becomes more challenging and demanding. After implementation of the corrective and improvement actions, high leakage current occurrence was reduced from baseline of 5784 ppm to 1567 ppm, better than the six sigma goal of 4715 ppm. Continuous improvement enhances the quality of the product, which also lowers the risk of having potential customer complaint in the future.*

***Keywords*—** *Semiconductor, QFN, IC, leakage current, ESD.*

I. INTRODUCTION

One important goal in semiconductor manufacturing industry is to deliver excellent quality products through innovative, fast, and cost-effective solutions, to have a very good impression from the customer. This is also one of the biggest challenges for any semiconductor company in order to maintain its competitive market position and value. Conversely, failure to provide customer expectation will result to possible business failure.

Semiconductor manufacturing industries offer vast range of semiconductor Integrated Circuits (IC) packages for different kinds of applications, ranging from automotive, consumer electronics, industrial, Internet of Things (IoT), Artificial Intelligence (AI), and many more. One particular semiconductor IC package is the Quad-Flat No-leads Multi-Row (QFN-mr) leadframe device being used as motor controllers on hard disk drives. The device (hereinafter referred to as Device P) is designed with Advanced Bipolar-CMOS-DMOS (BCD8) technology and packaged on QFN-mr platform utilizing a tapeless leadframe technology. As the die technology scales down, circuit metallization also becomes smaller. In turn, the device or package becomes more sensitive and susceptible to Electrostatic Discharge (ESD) and/or Electrical Overstress (EOS) damage. Presence of static charges, improper grounding, speed of material separation, and triboelectric charging (or simply tribocharging) could cause ESD damage to ESD-sensitive device. Fundamentals of ESD and ESD-related damage are discussed in details in the EOS/ESD Association references [1], [2]. As the product time-to-market becomes more demanding and challenging, there is a great drive to resolve package-related issues at the soonest as possible.

A. Semiconductor IC Package Defect in Focus

Parametric Parts Average Testing (PPAT) on leakage current response was employed at the Final Test to filter or screen-out units that are outliers (above 5-sigma) based on a reference distribution. Fig. 1 shows the outliers on 1 lot of Device P. The reference distribution is obtained on the response of the first 50 units tested at the Final Test.

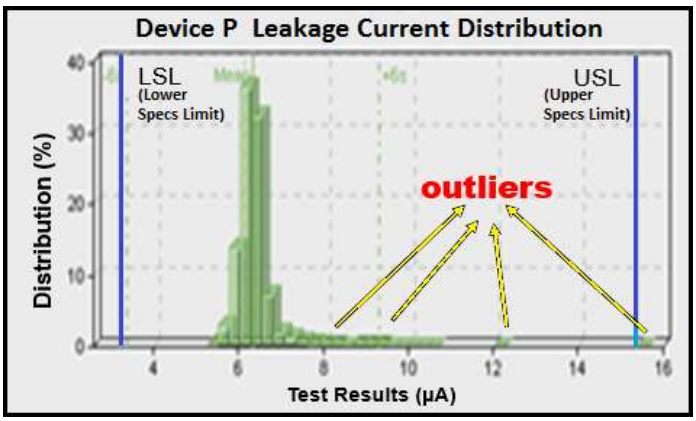

Fig. 1. Leakage current PPAT response, showing the outliers.

Note that it is of high importance to reduce the leakage current failures to ensure the product quality. If the leaky unit/device is functioning, that leaky connection will eventually degrade and become open-circuit and eventually disabling the functionality of the device.

Most of the rejections do not manifest any abnormality after Failure Analysis (FA) since the leakage current readings are still within the defined specification limits. However, the units are considered failing since they are outliers from the PPAT testing. For units above the specification limit, FA showed burnt metallization as shown in Fig. 2. This defect manifestation could be caused by an EOS/ESD issue.

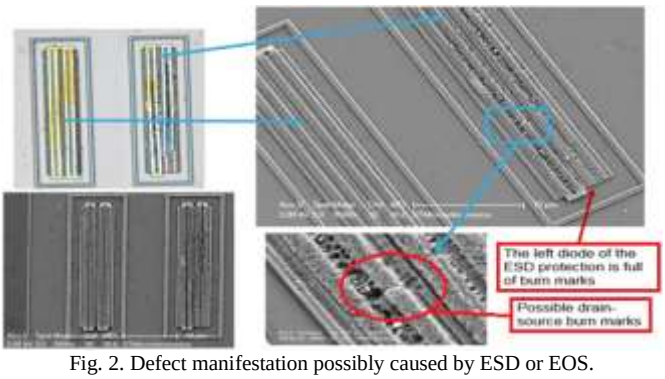

Fig. 2. Defect manifestation possibly caused by ESD or EOS.

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B. *Defect Ppm Baseline and Six Sigma Goal*

Baseline is initially computed to be at 5784 ppm. With entitlement of 4257 ppm, the calculated Six Sigma Goal is at 4715 ppm (70% improvement), as illustrated in Fig. 3.

The lots processed on workweek 1625 to 1626 showed that most of the defectives lie on 0.57% and the long term sigma (current process capability) was calculated to be at 2.5309. Fig. 4 shows the Device P current process capability.

C. *Objective Statement*

From the calculations shown earlier, the objective is to ultimately reduce the leakage current rejections from 5784 average ppm to 4715 ppm or even lower. As previously emphasized, it is of high importance to reduce or eliminate the occurrence of leakage current failures to ensure the product quality. Leaky units will eventually degrade and affect the performance the device.

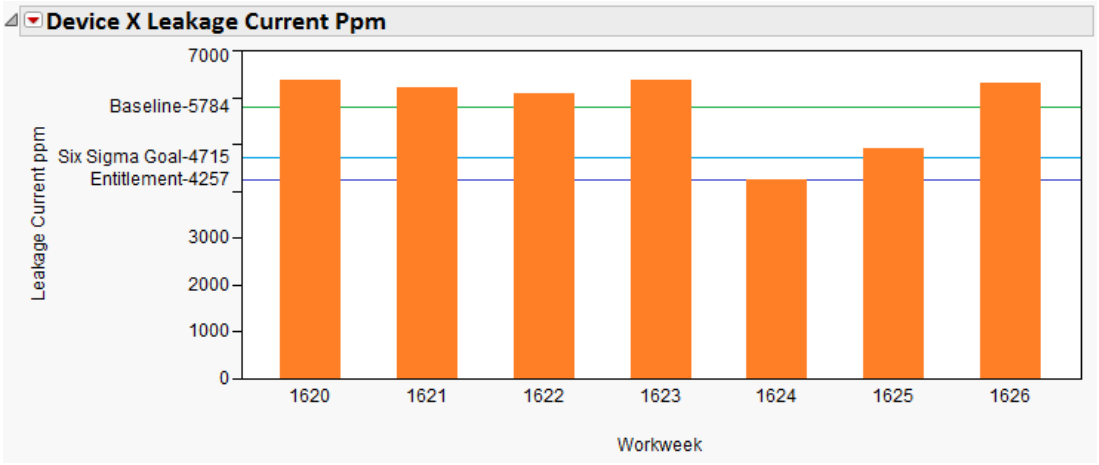

Fig. 3. Baseline and six sigma goal.

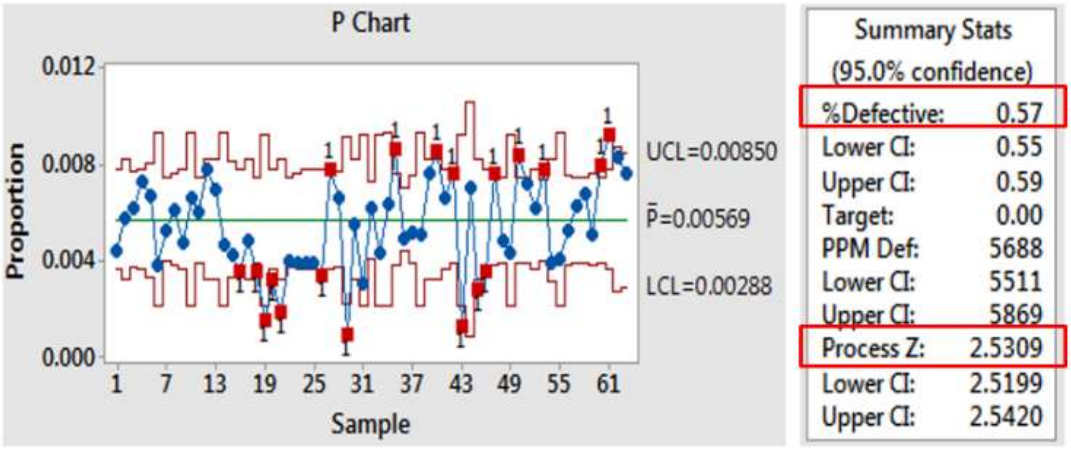

Fig. 4. Current process capability.

II. Review of Related Literature

From literature studies, known causes of high leakage current rejections and damaged metallization related to assembly manufacturing are summarized as:

- Electrostatic damage to sensitive devices [1], [2]
- Metallization damage brought by plasma charging [3]
- Tribocharging effects due to high waterjet parameters [4] [5], [6]
- High moisture content after waterjet process [4], [5], [7]
- High wafer saw transfer arm speeds and high water resistivity [6], [8]
- Trapped charges on high resistivity mold compounds [9]

Electrostatic discharge damage to units can be explained by three models [2], [7] given in Fig. 5.

A study [3] showed that plasma process with high cleaning parameters resulted to damage gate oxide, as illustrated in Fig. 6.

Triboelectric charging (or tribocharging) effects brought by high waterjet deflash parameters were also studied [4], [5], [7]. Lower waterjet pressure and temperature resulted to lower supply current failures. Some of the failures were also recovered after subjecting the units to baking which removed the package moisture content.

Wafer saw process could also contribute to the device's susceptibility to ESD damage. Processing without carbon dioxide (CO_2) bubbler and ionizer showed higher discharge voltage at around 18kV [6] as compared to a saw process with the required accessories, as shown in Fig. 7. Additional study showed that faster transport speed of 300m/s during wafer

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transfer at wafer saw station resulted to higher discharge voltage than that of a slower 5mm/s transport speed [6] [8].

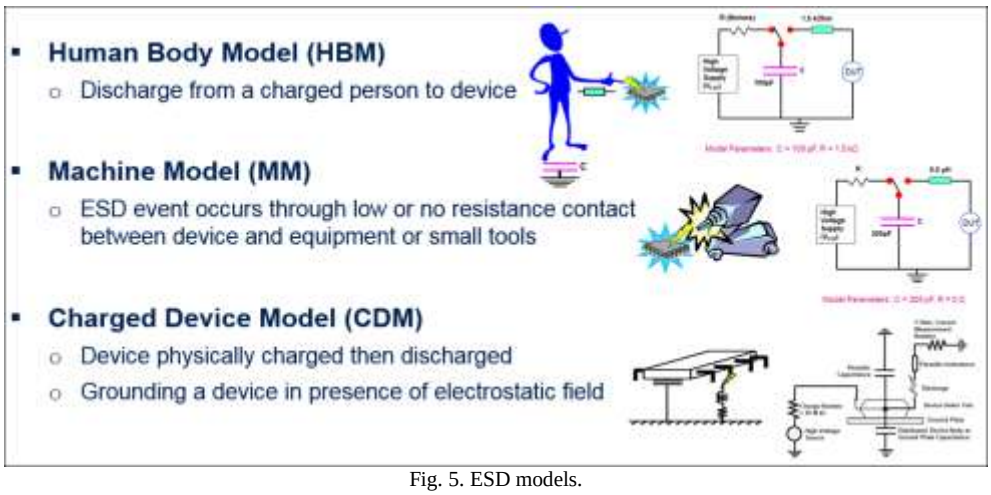

Fig. 5. ESD models.

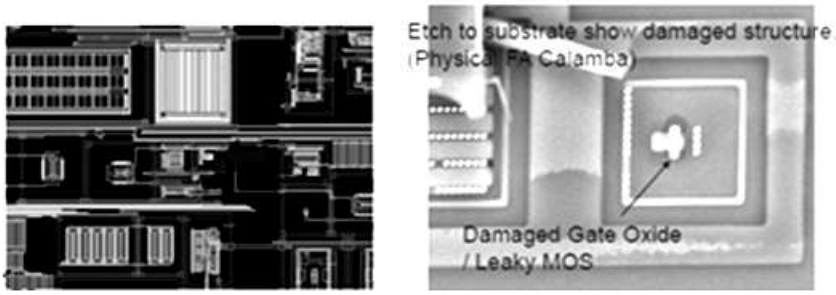

Fig. 6. Damage gate oxide with plasma process [3].

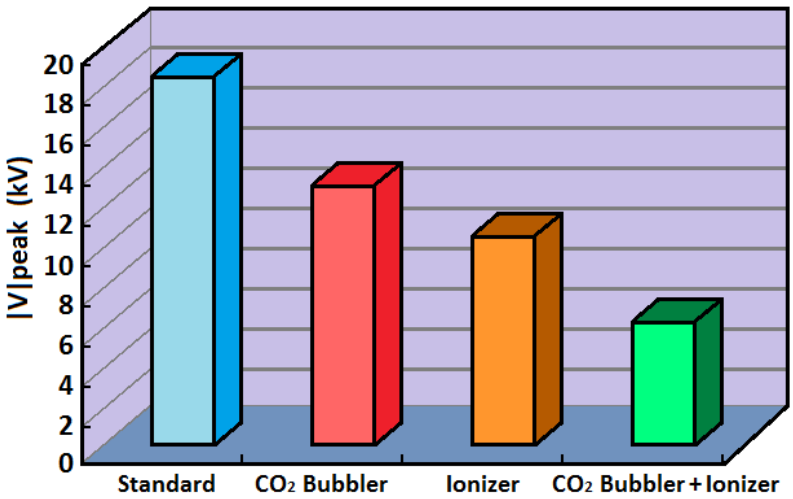

Fig. 7. Discharge voltage at wafer saw process [6].

Previous study also showed that leakage current was experienced on some molding compounds due to thermally induce trapped charge failure mechanism [9].

III. METHODOLOGY

A macro map was checked to determine the project scope. All process stations were investigated since all of these steps could induce ESD damage to the units (possible failure mechanism). Note that process flow may vary depending on the product and the technology [10-12]. For Device P, the process flow is shown in Fig. 8.

Multi-Vari analysis was carried out to determine which process step or equipment is contributing to higher rejections. It was found out that one diebond machine is causing higher leakage current rejections, as shown in Fig. 9. Investigation showed that there were ESD Events (> 1kV) on Diebonder 1. The machine was then subjected to health check and the ESD

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events were zeroed out by grounding the machine floating parts.

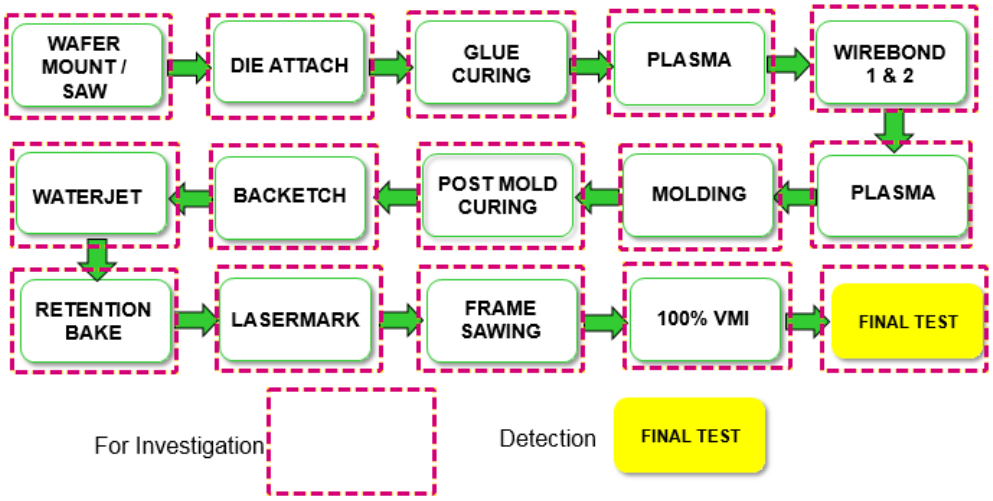

Fig. 8. Process flow.

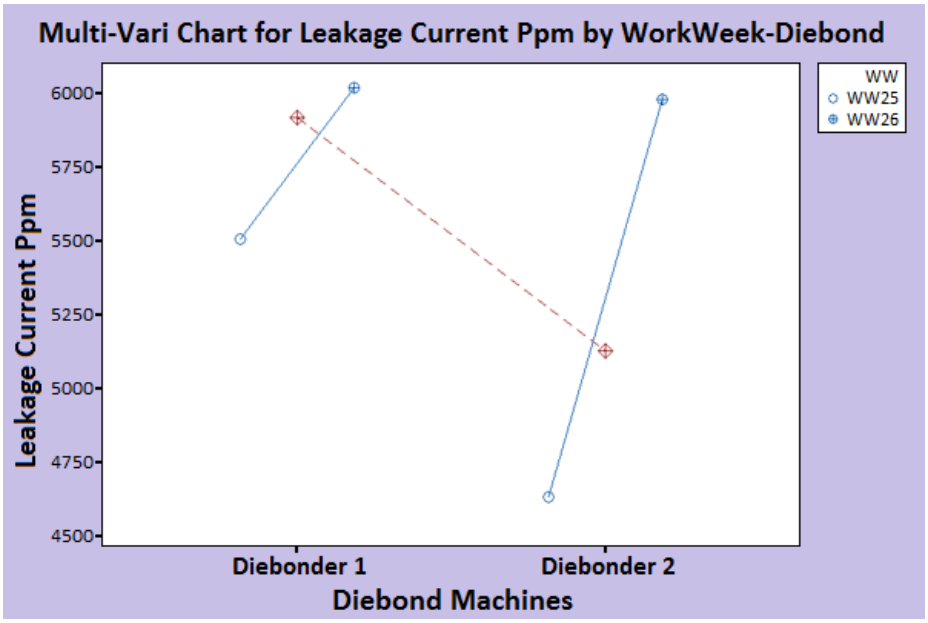

Fig. 9. Multi-vari analysis on diebond machines.

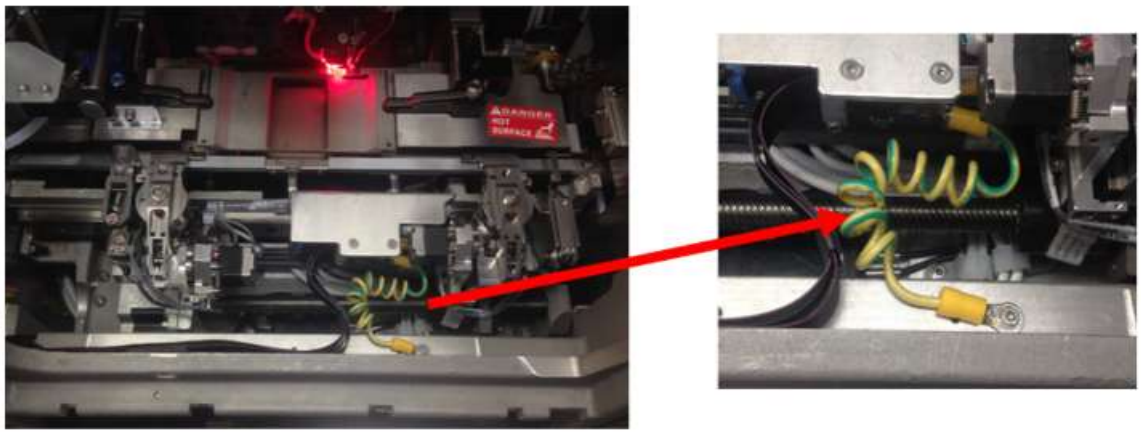

Fig. 10. Wirebond workholder machine grounding.

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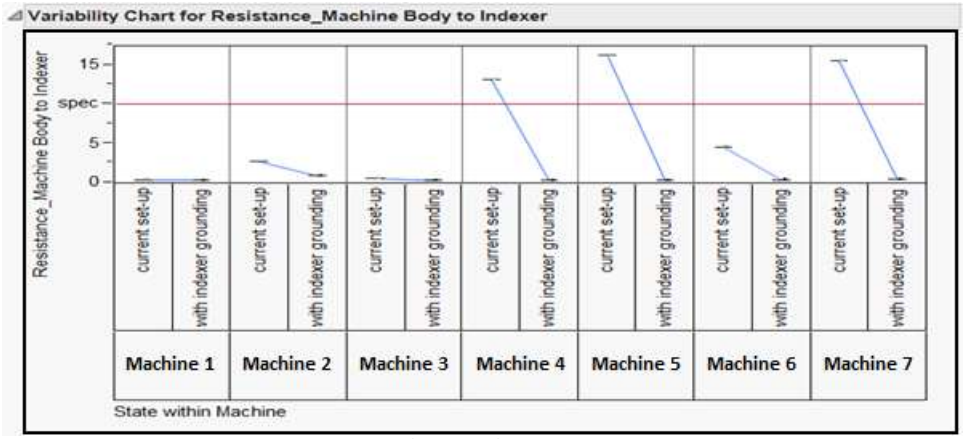

Fig. 11. Resistance reading, before and after implementing machine grounding.

With the findings, ESD events were checked in all process steps and equipment. Machine grounding from all process steps were checked and the ones failing were corrected. Fig. 10 illustrates wirebond workholder's grounding connected to its machine body.

Connecting the workholder to the machine body reduced the resistance level to less than 10Ω. Fig. 11 shows the resistance readings after grounding the workholder (current set-up vs with workholder indexer grounding).

IV. Results and Analysis

After implementation of the corrective and improvement actions, leakage current occurrence greatly reduced from a baseline of 5784 ppm to average of 1567 ppm last workweek 1627-29, as shown in Fig. 12. This is significantly better than the target performance at 4715 ppm.

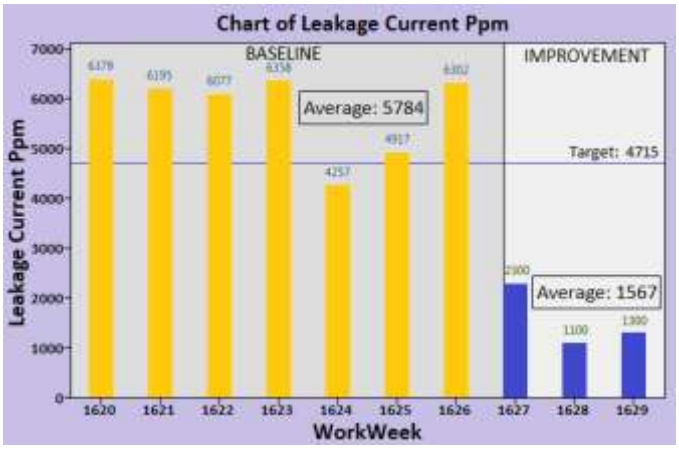

Fig. 12. Leakage current ppm improvement.

Specifications such as Failure Mode and Effects Analysis (FMEA) Control Plan, and Work Instructions were updated based on the findings and the corrective and improvement actions done. It is of high importance to make sure that proper grounding is installed in all machines. This is to ensure that any static charges and/or any charge build-up on the machine will be dissipated or discharged to ground through the metal components and the machine body.

V. Conclusion and Recommendations

Leakage current performance was significantly improved by eliminating ESD events through grounding of floating machine parts, maintaining the acceptable resistance value according to the specifications, and sustaining ESD controls. The leakage current occurrence decreased from a baseline of 5784 ppm to 1567 ppm after implementation of the improvement and corrective actions. This was achieved taking into account the motivation to deliver quality products given the challenging market cycle time.

Continuous improvement is important for sustaining the quality excellence of any product and of the assembly plant. One opportunity for further improvement is the optimization of the CO_2 bubbler and explore its resistivity settings so as to reduce the CO_2 consumption, at the waterjet deflash station [5].

VI. Acknowledgment

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