

Increasing Router Efficiency by Parallel Buffering and Packet Clustering Techniques

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Abstract— To increase the efficiency of the router at the high bandwidth usage paths in the network by adopting two techniques that are packet parallel buffering and packet clustering methods. In parallel buffering method we use high speed RAM memories to increase the packet buffer memory and these memory areas are divided parallel into 4 queue paths. Each queue received same amount of packets to the buffer area. We accommodate high income of data into the router buffer by using packet clustering method in router. For faster and efficient routing maximum number of packets are buffered into the router buffer. The buffered packets are randomly collected from buffers queue and that are accessed via both normal and packet clustering method. Here the packets of similar network are grouped into the minimum of 256 threshold size and cumulative packets are sent at once using normal routing.

Keywords— SRAM/ DRAM, parallel buffer, hybrid DRAM, router memory.

I. INTRODUCTION

Networking is the process of supplying data and information by linking the group of networks using hardware's. A hardware that are switches, hubs gateways, access points, network interface cards, networking cables, etc. that are more specific in networking. The tools that are required for communication and data processing in the network are all computer peripherals, computers and interface cards. The most common kind of networking in hardware is a copper-based Ethernet adapter because of its standard inclusion on most modern computer systems. Wireless networking has, however, become increasingly popular, especially for portable and handheld devices. Other hardware prevalent in computer networking includes data center equipment (such as file servers, database servers and storage areas), network services (such as DNS, DHCP, email, etc.) as well as devices which assure content delivery. The phenomenal growth of the internet has been fueled by the rapid increase in the communication link bandwidth. Internet routers play a crucial role in sustaining the growth by being able to switch packets extremely fast to keep up with growing bandwidth. This demands sophisticated packet switching and buffering techniques. Packet buffers need to be designed to support large capacity, multiple queues, and provide short response time.

II. BACKGROUND AND RELATED WORK

A. SRAM and DRAM Technology

Current SRAM and DRAM cannot individually meet the access time and capacity requirements of router buffer. While SRAM is fast enough with an access time of around 2.5ns, its

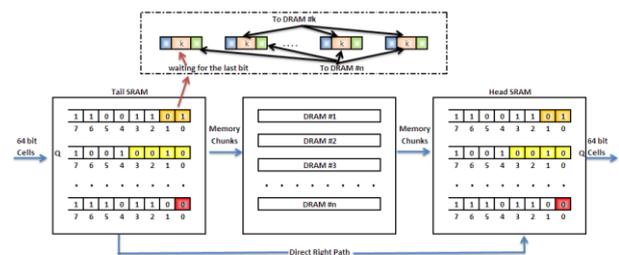
larger size is limited by current technologies to only a few MB. On the other hand, a DRAM can be build up with large capacity, but the typical memory access time is too large, around 40ns.

B. Packet Buffer

Bridging the speed gap between the SRAM and DRAM becomes a major challenge. This speed mismatch does not refer to the bandwidth but the access time and the concomitant access granularity. Due to the variable packet size that the IP protocol allows, it is common for packet processor to segment packets into fixed size cells to make them easier to manage and switch. A common choice for the cell size is 64 bytes because it is the first power of two larger than the size of minimum packet. For designing packet buffer we need to maintain multiple queues, rather than a single FIFO queue. Is used to find an efficient way to bridge the gap of size between the call and the chunk

III. PROBLEM IN EXISTING ROUTER

The router buffer sizing is still an open issue. The traditional rule of thumb for internet routers states that the routers should be capable of buffering $RTT \cdot R$ data, Where RTT is a round-trip time for flows passing through the router, and R is the line rate. Many researchers claimed that the size of buffers in backbone routers can be made very small at the expense of a small loss in throughput. To avoid $RTT \cdot R$ the researchers are used "Traffic-aware" approach which aims to provide different services for different types of data streams. But this approach also the packets are accumulated at the buffer until its being full, the extra packet that comes to the router always fail to get into router.



IV. SCOPE OF THE PROJECT

Our research relates to increase the efficiency of the router in high bandwidth usage paths. Our scenario increases the efficiency by using two techniques.

A. Packet parallel Buffer

B. Packet clustering

A. Packet Parallel Buffer

To increase effective bandwidth, designers move to new buffering architecture, called the parallel packet buffering (PPB), which increases the effective memory bandwidth significantly. In an high speed networking design architecture needs to buffer the incoming packets at the line rate. Then the buffered packets are forwarded to appropriate ports at the line rate. The following equation demonstrates the bandwidth measure

$$A = 1 - \frac{1}{LR} \times \left(1 - \exp\left(\frac{-k \times D}{D - n}\right) \right) \times 100$$

LR – Line rate of single Memory based Buffer

D – Data width of PPB

K – Constant depend on LR and D

B. Packet Clustering

Packet clustering is the process of grouping the same port data's together. The goal of clustering is to discover new set of categories. In packet clustering partitioning method relocate the moving instances from on cluster to another cluster.

V. PROPOSED ARCHITECTURE

In this paper we suggest gns3 Beowulf clustering method to group the buffered data. Older days routers are used SRAM/DRAM technology. Here we design a new router topology for buffer the data from the packet parallel buffer. We design a router with 4 segments, each segment will buffer a packets from the parallel buffer with minimum of 256 threshold size in each cluster

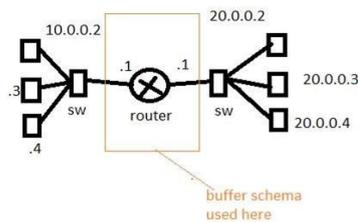


Fig. 1. Sample network topology

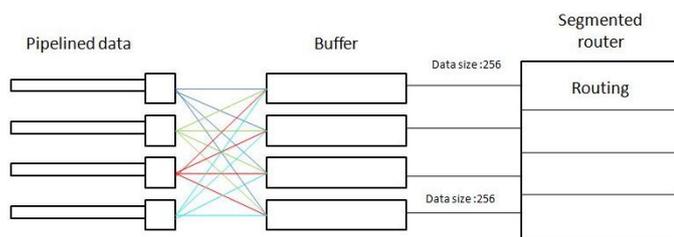


Fig. 2. Proposed architecture

VI. SIMULATION ANALYSIS

In a simulation purpose we use GNS3 as a simulator to analysis the performance of the topology. In GNS3 many supporting analysis tools are used that are wire shark and solar wind technologies.

A. GNS3 Beowulf Cluster

In our project we use Beowulf cluster, the code that written and designed in MPI code and messages. It called “Parallel Programming”, that allow user to run the single program on multiple computers. In a running method some parts of the code or data packet runs on single Personal computer while other parts run on other personal computer in the cluster.

VII. CONCLUSION

To avoid the packet loss with efficient router design. In this proposed system the memory of the buffer is complimented with the secondary fast memory of RAM (SRAM), which is dived into segments of Four equal data structures and the operating system of the router is allows to collect the packets into four ports simultaneously, collect into the buffer catch and also the four queue memory of the router.

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