International Research Journal of Advanced Engineering and Science
ISSN: 2455-9024

Performance Comparision of Carry Select Adders

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Abstract—*Adder is a digital circuit that performs addition of numbers. To perform fast arithmetic operations, carry select adder (CSLA) is one of the fastest adders used in many data-processing processors. The structure of CSLA is such that there is further scope of reducing the area, delay and power consumption. Simple and efficient gate – level modification is used in order to reduce the area, delay and power of CSLA. Based on the modifications, 8-bit, 16-bit, 32-bit architectures of CSLA are designed and compared. In this paper, conventional CSLA is compared with Modified Carry select adder (MCSLA) and proposed CSLA, in terms of area, delay and power consumption. The result analysis shows that the proposed structure is better than the conventional CSLA.*

Keywords— *Adder, carry select adder (CSLA), modified CSLA (MCSLA), proposed CSLA (CSLA), data processing processors.*

I. INTRODUCTION

Adders are not only used in the arithmetic logic unit, but also in other parts of the processor, where they are used to calculate addresses, table indices and similar applications. Some other applications of adders are in Multiply – Accumulate (MAC) structures. Adders are also used in multipliers, in high speed integrated circuits and in digital signal processing to execute various algorithms like FFT, IIR and FIR. Now a days, design of low power, area efficient high speed data path logic systems are the most substantial areas in the research of VLSI design. On the basis of requirements such as area, delay and power consumption some of the complex adders are Ripple Carry Adder, Carry look-Ahead Adder and Carry Select Adder. Ripple Carry Adder (RCA) shows the compact design but their computation time is longer. Time critical applications make use of Carry Look-Ahead Adder (CLA) to derive fast results but it leads to increase in area. But the carry select adder provides a compromise between the small areas but longer delay of RCA and large area with small delay of Carry Look Ahead adder [1] This paper presents a comparative analysis of various adders and proposed design of CSLA by sharing Common Boolean Logic and modified CSLA using Binary to Excess-1 Converter (BEC). Both these adders show less area, delay and power than other adders.

This paper is organized as follows: In section I Types of adders is shown, section A. deals with Ripple Carry Adder section B. deals with modified CSLA, section C. explains about Proposed CSLA using common Boolean logic. II Results are analyzed in section III and Conclusion in section VI.

II. ADDERS

A. Ripple Carry Adder

Ripple Carry Adder consists of cascaded ―N‖ single bit full adders. Output carry of previous adder becomes the input carry of next full adder. Therefore, the carry of this adder traverses longest path called worst case delay path through N stages. Figure 1 shows the block diagram of ripple carry adder. Now as the value of N increases, delay of adder will also increase in a linear way. Therefore, RCA has the lowest speed amongst all the adders because of large propagation delay but it occupies the least area.

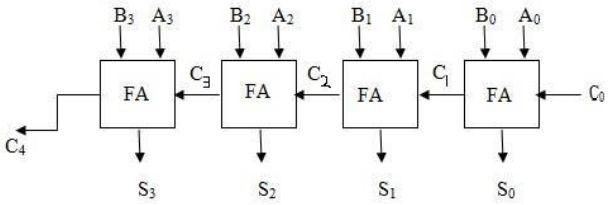

Fig. 1. 4-bit ripple carry adder

The basic idea of this work is to use Binary to Excess- 1 converter (BEC) instead of RCA with Cin=1 in conventional CSLA in order to reduce the area and power. [2], [3] BEC uses less number of logic gates than N-bit full adder structure. To replace N-bit RCA, an N+1 bit BEC is required. Therefore, Modified CSLA has low power and less area than conventional CSLA. CSLA has been chosen for comparison with modified design using BEC as it has more balanced delay, less area and low power [4]. Regular CSLA also uses dual RCAs. In order to reduce the area and power, the design is modified by using BEC instead of RCA with Cin=1. Therefore, the modified CSLA occupies less area and low power. Further also, the parameters like delay, area and power can be reduced

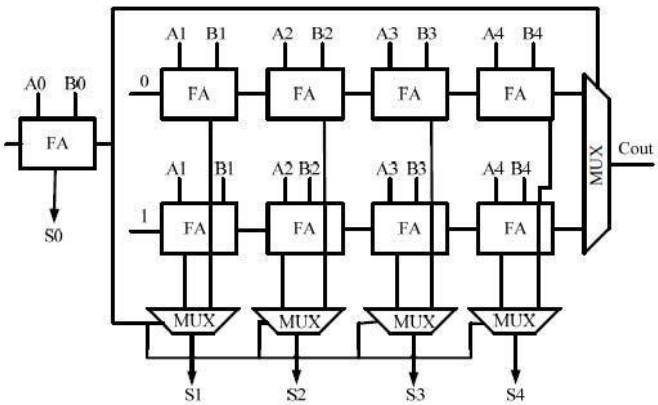

Fig. 2. Conventional carry select adder

Nithin Bidare Puttaraju and Adithya, "Performance comparision of carry select adders," *International Research Journal of Advanced Engineering and Science*, Volume 1, Issue 2, pp. 73-75, 2016.

International Research Journal of Advanced Engineering and Science
ISSN: 2455-9024

By sharing Common Boolean Logic (CBL), a circuit of CSLA is proposed. This proposed design is better than all the other adders in respect of area, delay and power consumption

B. *Modified CSLA*

The main idea of this work is to use BEC instead of RC with carry Cin=1 in order to reduce the area and power of conventional CSLA. BEC [3] is a circuit used to add 1 to the input numbers. Circuit of BEC as shown in figure 3. Goal of addition is achieved using BEC together with the multiplexer as shown in figure 4.One of the input of 8:4 MUX gets as its inputs(B3,B2,B1andB0) and another input of MUX is BEC output. Boolean expressions of 4-bit BEC are listed below

X0=~B0
X1= B0^B1
X2=B2^(B0&B1)
X3=B3^(B0&B1&B2)

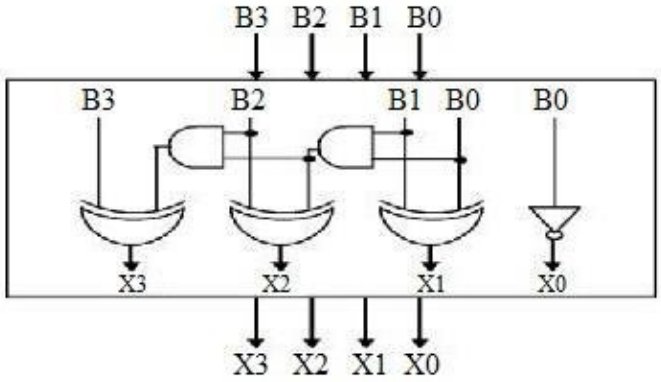

Fig. 3. 4-bit binary to excess-1 converter

The main idea of this work is to use BEC instead of RCA with Cin=1 in order to get the reduced area and power consumption of the conventional CSLA. To replace the Nbit RCA, N+1 bit BEC is required

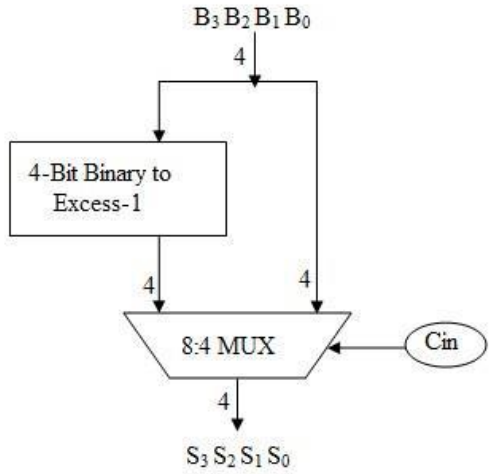

Fig. 4. 4-bit binary to excess-1 logic with 8:4 multiplexer

Thus, modified CSLA is designed such that it occupies less area and has low power than conventional CSLA.

C. *Proposed CSLA Using Common Boolean Logic*

To remove the duplicate adder cells in the conventional CSLA, an area efficient CSLA is proposed by sharing Common Boolean Logic (CBL) term as shown in figure 5.The truth table shown in table I of a single-bit full-adder indicates that output sum (S0) is Ex-OR of inputs A and B when carry initial is logic ―0‖ while output S0 is Ex-NOR of inputs A and B when carry initial is logic ―1‖ as illustrate as two red circles in truth table. The improved CSA can be implemented by using this technique of sharing the common Boolean logic term in summation generation.

TABLE I. Truth table of single bit full adder, where the upper half part is the case of Cin=0 and the lower half part is the case of Cin=1

Cin	A	B	S0	C0
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

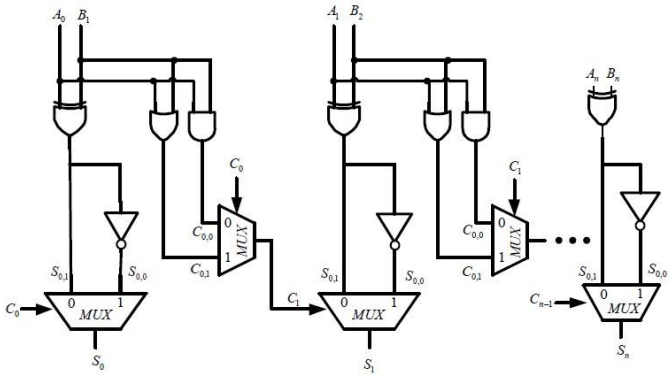

Fig. 5. Internal structure of the proposed area-efficient carry select adder is constructed by sharing the common Boolean logic term

Hence we need to use Ex-OR gate and INV gate to generate the output sum signal pair. Sum output either the Ex-OR or the Ex-NOR could be selected using the multiplexer with select line as previous carry signal. The truth table also reveals that output carry (C0) is AND of A, B inputs when initial carry is logic ―0‖ while C0 is OR of A, B when initial carry is logic ―1‖.Same previous carry as select line to second multiplexer is used to select the carry output of the first stage which would act as select line of the multiplexers in the second stage. As both sum generation and carry generation is carried out in parallel therefore there exist some competitiveness in speed also the power consumption reduces as duplication of the hardware doesn't exist in improved CSA as in case of the conventional This method replaces the Binary

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to Excess-1 converter add one circuit by common Boolean logic. As compared with modified CSLA, the proposed structure is little bit faster. Internal structure of proposed CSLA is shown in figure 5.

III. RESULT

Model	Area	Power	Delay
CSLA	129.8	48289.875nw	43.311ns
Modified CSLA	909	79.81MILIW	42.65 NS
Proposed CSLA	835	18387.119nw	44.36NS

IV. CONCULSION

The radix-8 multiplier is designed by using Carry Select Adder, Modified Carry Select Adder and Proposed CSLA Using Common Boolean Logic, and area occupied is compared with Carry Select Adder, Modified Carry Select Adder and Proposed CSLA Using Common Boolean Logic Among these three designs adders using CSLA Using Common Boolean Logic is having less area occupied than compared to adders using Carry Select Adder, Modified Carry Select Adder The propagation delay can be further reduced by using different combination of adders and also work can be done to reduce the area occupied and power dissipation.

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